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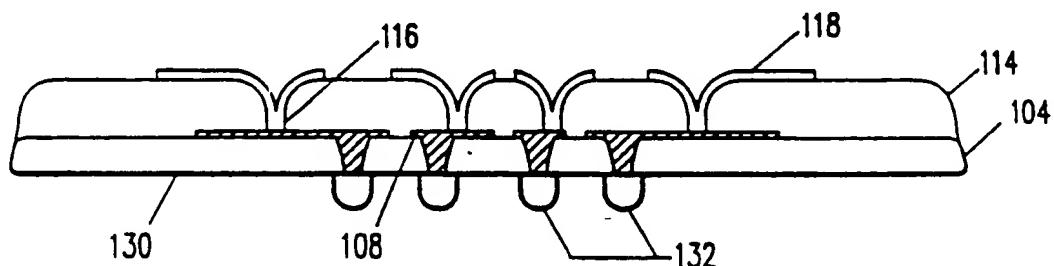
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(54) Title: MAKING AND TESTING AN INTEGRATED CIRCUIT USING HIGH DENSITY PROBE POINTS



## (57) Abstract

Each transistor or logic unit on an integrated circuit wafer (1) is tested prior to interconnect metallization. By means of CAD software, the transistor or logic units placement net list is revised to substitute redundant defect-free logic units for defective ones. Then the interconnect metallization is laid down and patterned under control of a CAD computer system. Each die in the wafer thus has its own interconnect scheme, although each die is functionally equivalent, and yields are much higher than with conventional testing at the completed circuit level. The individual transistor or logic unit testing is accomplished by specially fabricated flexible tester surface (10) made in one embodiment of several layers of flexible silicon dioxide, each layer containing vias and conductive traces leading to thousands of microscopic metal probe points (15-1, 15-2) on one side of the test surface (10). The probe points (330) electrically contact the contacts (2-1, 2-2) on the wafer (1) under test by fluid pressure.

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1                   "MAKING AND TESTING AN INTEGRATED CIRCUIT  
2                   USING HIGH DENSITY PROBE POINTS"

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8 CROSS REFERENCE TO PRIOR APPLICATION

9                   This is a continuation-in-part application of U.S.  
10 Patent Application Serial No. 07/194,596, filed May 16, 1988  
11 issued as U.S. Patent No. 4,924,589.

12

13 BACKGROUND OF THE INVENTION

14 Field of the Invention

15                   This invention relates to a method of making and testing  
16 integrated circuits, and a device used to perform such  
17 testing.

18

19 Description of the Prior Art

20                   Integrated circuits (ICs) comprise active and passive  
21 elements such as transistors, diodes, resistors, and  
22 capacitors, that are interconnected in a predetermined  
23 pattern to perform desired functions. The interconnections  
24 are effectuated by means of metallization layers and vias.  
25                   A "via" is a hole through an insulation layer in which  
26 conductor material is located to electrically interconnect  
27 one conductive layer to another or to an active or passive  
28 region in the underlying semiconductor substrate. Present  
29 day technology generally employs two metallization layers  
30 that are superimposed over the semiconductor wafer  
31 structure. Integrated circuits and assemblies have become  
32 more complex with time and in a logic circuit, the number of  
33 integrated circuit logic units (ICLUs) and interconnects on  
34 a given size die have been substantially increased  
35 reflecting improved semiconductor processing technology. An  
36 ICLU can be a device (such as a transistor), a gate (several  
37 transistors) or as many as 25 or more transistors and other  
38 devices. As is well known in the art, these conductive

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1 contact points have a typical center-to-center spacing of  
2 about 6 to 15 microns ( $\mu\text{m}$ ).

3 Standard processing to make logic structures (e.g., gate  
4 arrays) includes first fabricating as many as half a million  
5 transistors comprising a quarter of a million gates per  
6 die. Each semiconductor wafer (typically silicon but  
7 sometimes of other material such as gallium arsenide)  
8 includes many die, for example, several hundred. In one  
9 type of gate array, for example, the transistors are arrayed  
10 in rows and columns on each die, and each transistor is  
11 provided with conductive contact points (typically metal but  
12 sometimes formed of other conductive material such as poly-  
13 crystalline silicon), also arrayed in rows and columns.

14 In the prior art, the next step is to use fixed masks to  
15 fabricate the conductive layers (sometimes called  
16 "metallization layers"), to connect together the individual  
17 gate-array devices. Typically two or sometimes three metal-  
18 lization layers are used.

19 After this, the completed die is tested. If any of the  
20 devices on the die are defective, that die will fail an  
21 exhaustive test and be scrapped. Therefore, the more  
22 transistors per die the lower the manufacturing yield. In  
23 some cases redundant sections of a circuit are provided that  
24 can be substituted for defective sections of a circuit by  
25 fuses after metallization. Typically such redundant  
26 sections can be 5% to 10% of the total circuit.

27

28 SUMMARY OF THE INVENTION

29 An object of this invention is to provide an improved  
30 test procedure for integrated circuits to increase  
31 production yields, by testing a circuit at the ICLU level  
32 (hereinafter called "fine grain testing"), compared to  
33 conventional testing at the functional IC or die level.

34 Another object is to permit the fabrication of very  
35 large integrated circuits, in terms of the number of ICLUs  
36 or devices per circuit.

37 The present invention improves on prior art by testing  
38 each ICLU prior to metallization. Redundant ICLUs ar

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1 provided on the die to substitute for those found to have  
2 defects. Then the metallization layers are fabricated so as  
3 to exclude defective ICLUs and substitute good ones from the  
4 redundant group and render the circuit operable. The  
5 present invention uses a fine grain testing approach, by  
6 testing at a low level of complexity.

7 One key to the present invention is a specially  
8 fabricated flexible test means made of flexible silicon  
9 dioxide in one embodiment and including multi-layer metal  
10 interconnects and microscopic test points. The flexible  
11 tester means includes a tester surface, connected to test  
12 equipment, that permits testing of each device. Then by CAD  
13 (computer aided design) means, each die is metallized and  
14 the metal layer is patterned by suitable means, such as  
15 E-beam and Ion-Beam processing, to fabricate discretionary  
16 metallization interconnect layers of individual gate array  
17 devices.

18 The tester surface is formed on a standard silicon wafer  
19 typically by means of a low stress chemical vapor deposition  
20 process. The tester surface includes its own metallization  
21 layers. On one side of the tester surface are thousands of  
22 probe points to contact the contact points on the wafer  
23 under test. The tester surface is a special flexible form  
24 of silicon dioxide which can be pressed flexibly against the  
25 wafer under test to achieve good electrical contact.

26 By eliminating defects at the device level, process  
27 yield is vastly increased -- for example to about 90%  
28 regardless of die size, in contrast to much lower yields  
29 using prior art technology. The present invention also  
30 allows successful fabrication of very large die compared to  
31 conventional technology.

32

33 BRIEF DESCRIPTION OF THE DRAWING

34 Fig. 1 shows a section of a gate array wafer and the  
35 device contacts.

36 Figs. 2-3 show a top and side view of part of the tester  
37 surface.

38 Figs. 4(a) and 4(b) show the test procedure.

1       Fig. 5 shows the fluid pressure test assembly.

2       Fig. 6 shows an exploded view of the wafer and tester  
3 surface.

4       Figs. 7-12 show the steps to fabricate the tester  
5 surface.

6       Figs. 13-15 show the steps to fabricate another  
7 embodiment of the tester surface.

8       Fig. 16 shows how nine die can form one super die.

9       Figure 17(a) shows a tester surface.

10      Figures 17(b) to 26 show various probe point structures.

11      Figures 27(a) to 27(h), 28(a) to 28(h), and 29 show  
12 fabrication of probe points.

13      Figures 30, 31 show tester surfaces.

14      Figure 32 shows an active matrix probe point surface.

15      Figure 33 shows a polysilicon film for a flexible tester  
16 surface.

17      Figures 34, 35 show tester head assemblies.

18      Figures 36 to 41 show discretionary patterning for IC  
19 fabrication.

20      Figures 42(a) to 42(d) show repair of IC traces.

21      Each reference numeral when used in more than one Figure  
22 refers to the same or a similar structure.

23

24      DETAILED DESCRIPTION

25      As stated above, the prior art fabricates a plurality of  
26 transistors on a die, interconnects the transistors to form  
27 desired logic, tests the entire die, and scraps the die if  
28 the logic doesn't work. In the present invention, after  
29 fabricating the transistors exactly as before, the  
30 transistors or ICLUs are tested individually. Then the  
31 interconnect scheme is modified, if necessary, by CAD means  
32 (of well known design) to bypass defective transistors or  
33 ICLUs and substitute, logically speaking, replacement  
34 ICLUs. Then the metallization layers are deposited, and  
35 patterned in accordance with the modified interconnect  
36 scheme typically by E-beam (Electron-beam) lithography,  
37 instead of the masking process of the usual conventional  
38 technology. Thus each die has its own unique interconnect

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1 scheme, even though each die is to carry out the same  
2 function as the other die.

3       The present invention in one embodiment begins with a  
4 gate array conventionally fabricated on a silicon or GaAs  
5 wafer. The gate array transistors are arrayed in columns  
6 and rows on the wafer surface 1, and the active regions of  
7 each transistor are provided with contact points such as 2-1  
8 to 2-32 which are in columns and rows also as shown in  
9 Figure 1 (not all contact points are numbered). Redundant  
10 (or extra) devices are designed into each column, with a  
11 redundancy factor dependent on the expected yield of the  
12 individual transistors or ICLUs being tested.

13       The surface of the wafer 1 is optionally planarized with  
14 a cured layer of polyimide 0.8 to 1.5 micron thick if the  
15 step heights between contact points are greater than 0.5  
16 microns. (The contact points 2-1 to 2-32 are masked from  
17 the polyimide layer, to create a via over each contact point  
18 free of polyimide, and metal is deposited to fill the via.)

19       The fabricated (but not metallized) wafer 1 is now ready  
20 for testing. In the described embodiment, only one column  
21 of transistors on each die is tested at a time, although  
22 testing more than one column per step is possible. For a  
23 die of typical complexity this requires making contact with  
24 all of the perhaps 10,000 or so contact points such as 2-1  
25 to 2-4 in one column simultaneously, and then stepping  
26 across all 100 or 200 or more columns in each die, to  
27 totally test each die in step-and-repeat fashion. Each  
28 contact point such as 2-1 is small - usually 4 X 4  
29 microns. Each wafer contains a plurality of die, the exact  
30 number depending on the size of the wafer but typically  
31 being in the hundreds.

32       The flexible tester of this invention includes a tester  
33 surface 10 (described in detail below) as seen in Fig. 2  
34 which includes a series of tester surface contact points  
35 including 15-1, 15-2 (which are arranged to contact on a  
36 one-to-one basis the corresponding contact points in a  
37 column on the die under test) and a complete wiring  
38 interconnection, including a testing array which includes

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1 contacts 16-1, 16-2 and 16-3 and interconnect pathways 17-1,  
2 17-2 and 17-3 as seen in Fig. 3, at various levels 22, 23,  
3 24 in the tester surface. The tester array which includes  
4 contacts 16-1, 16-2 and 16-3 connects to a conventional  
5 tester signal processor as shown in Fig. 4a having line  
6 driver logic circuits for accessing serially or in parallel  
7 the devices under test. The driver logic signals are  
8 programmed separately in a well known manner and are  
9 multiplexed between testing array contacts 16, providing  
10 programmable input/output means for supplying diagnostic  
11 signals to the transistors or ICLUs under test. Therefore,  
12 all the wafer contact points in one column can be accessed  
13 in one physical contact step of the transistors or devices  
14 to be tested.

15 The wafer 1 under test and the tester surface 10 are  
16 disposed on a support 26, as shown schematically in Fig.  
17 4(a), for test purposes, to electrically connect the contact  
18 points on the tester surface 10 and corresponding contact  
19 points on the wafer 1. Figure 4(b) shows the test procedure  
20 in process-flow format. A fluid well or bladder (not shown)  
21 is used to exert an uniform pressure over the flexible  
22 tester surface 10 (Fig. 4(a)) in order to conform it to the  
23 surface of the wafer 1 under test and to ensure that the  
24 numerous corresponding contact points on the tester surface  
25 10 and the wafer 1 come together and make firm electrical  
26 contact. This is possible due to the fact that the surface  
27 of the wafer 1 under test typically has a controlled total  
28 runout flatness within 6 to 10 microns across its complete  
29 surface. Secondly, the tester surface 10 is less than 15  
30 microns thick and typically 1.5 microns thick and of a very  
31 flexible material, such as low stress silicon dioxide.  
32 Thirdly, the metal contact points are the highest raised  
33 surface features on either the tester surface 10 or the  
34 surface of the wafer 1 under test, and are of a controlled  
35 uniform height typically between 2 and 6 microns.

36 The wafer 1 under test as shown in Fig. 4(a) is mounted  
37 on an x-y motion table (not shown). Movement of the table  
38 in the x-y directions positions the wafer for test by

1 alignment of the contact points such as 15-1 and 15-2 of the  
2 test surface 10 (Fig. 2) with the corresponding device  
3 contact points such as 2-1 and 2-2 of the wafer 1.

4 During the test procedure as shown in Fig. 4(a), the  
5 wafer 1 under test is retained by suction in a substantially  
6 planar fixed position, by means of the support 26  
7 illustrated in Fig. 4(a) and in Fig. 5. Use of suction to  
8 hold a wafer in place is well-known. Tester surface 10 is  
9 mounted on a support ring 36 (as described below) to provide  
10 mechanical support and electrical connections, as shown in  
11 Fig. 5. The tester surface 10 is urged uniformly toward the  
12 wafer 1 under test by a fluid well or bladder 38 immediately  
13 behind tester surface 10. A solenoid (not shown) is  
14 provided for macro control of the pressure exerted by the  
15 fluid in the fluid well 38 on tester surface 10. The depth  
16 of fluid well 38 is less than 100 mils; this is the distance  
17 between the back of tester surface 10 and piezoelectric  
18 pressure cell 40.

19 Piezoelectric pressure cell 40 is a layer of material  
20 about five-hundredths of an inch (one millimeter) thick that  
21 will expand about one-half micron when voltage is applied to  
22 the piezoelectric material. The applied pressure on the  
23 back of the tester surface 10 is only a few grams per square  
24 centimeter. Piezoelectric pressure cell 40 provides the  
25 last increment of pressure on the fluid and in turn on the  
26 back of tester surface 10 to achieve good electrical contact  
27 between the contact points such as 15-1 and 15-2 on tester  
28 surface 10 and the contact points such as 2-1 and 2-2 on  
29 wafer 1. The fluid is provided to the assembly through  
30 fluid port 46 which is connected to a fluid reservoir (not  
31 shown). The support ring 36 includes computer cabling  
32 attachment sites 48 and multiplexer circuits 50. The  
33 support ring structure is described in more detail below.  
34

35 As described above, mechanical positioners (i.e., x-y  
36 table aligners and conventional mechanical vertical  
37 positioners, not shown) bring the wafer 1 to within a few  
38 mils of the tester surface 10 and make a first approximation  
of the alignment of contact points through a conventional

1 optical aligner (not shown). The optical alignment is  
2 performed in a manner similar to that used by present  
3 semiconductor mask aligners, by using alignment patterns in  
4 predetermined positions on both the wafer 1 being tested and  
5 the tester surface 10. Only the pressure of the fluid moves  
6 the tester surface 10 the one or two mil distance separating  
7 the tester surface 10 and the wafer 1 to be tested in order  
8 to gain physical contact. Figure 6 illustrates in an  
9 exploded view wafer 1 and tester surface 10 being moved by  
10 fluid pressure from fluid well 38 just before wafer contact  
11 points such as 2-1 and 2-2 make contact with corresponding  
12 tester surface contacts such as 15-1 and 15-2.

13 In an additional alignment method, a small area (not  
14 shown) with a pattern of alignment contact points of various  
15 sizes up to 1 mil (25 microns) square and positioned at two  
16 or three corresponding alignment sites on both the wafer 1  
17 and the tester surface 10 is then used as an electrical  
18 circuit feedback system. The feedback system, starting with  
19 the largest contact points at each site and moving  
20 progressively to the smallest, determines the accuracy of  
21 the alignment and makes appropriate micron sized adjustments  
22 under computer control to within sub-micron x-y alignment  
23 accuracy.

24 In the described embodiment, the fluid in the test  
25 surface assembly is Florinert from DuPont. Any alternate  
26 fluid with similar nonconductive and nonreactive properties  
27 could be substituted.

28 After an entire wafer 1 has been tested, it is removed  
29 and another wafer moved into position to be tested.

30 The data resulting from the tester signal processor is a  
31 list of the location of each defective transistors or  
32 ICLUs. This list is automatically communicated to the  
33 conventional CAD means from the tester signal processor as  
34 shown in Fig. 4. The CAD means then, by special software  
35 algorithms works out an interconnect strategy for each  
36 die. Therefore, the master placement scheme of the net list  
37 is modified in terms of the placement of the defective ICLUs  
38 so as to bypass the defective ICLUs and interconnect defect-

1 free ICLUs from the stock of redundant ICLUs.

2 The invention uses two alternative software  
3 algorithms: recomputation of metallization trace routing or  
4 a CAD rip-up router.

5 The first alternative is the well-known and commercially  
6 available recomputation of the metallization trace routing  
7 for all affected layers of a specific IC after it has been  
8 tested. The routing is performed automatically with CAD  
9 software. This routing procedure requires that sufficient  
10 defect-free redundant ICLUs have been allocated in the  
11 master placement of ICLUs and that the redundant ICLUs can  
12 be routed into the circuit given the potential restrictions  
13 that the number of metallization layers may present. The  
14 software that precedes this processing performs the entry  
15 into a CAD system of the placement net-list change commands  
16 that direct the substitution of the defective ICLUs with  
17 available redundant ICLUs. These change commands are  
18 specific to the CAD system that is selected for use, and the  
19 commands issued are similar to those a circuit designer  
20 would enter if making an ICLU placement select in a design  
21 change when using a gate-array.

22 This recomputation routing approach makes substantial  
23 requirements on computing resources. However, super-  
24 minicomputers presently available are sufficient to meet the  
25 computational requirements.

26 The second software alternative, a CAD rip-up router,  
27 takes advantage of the knowledge that the defects occurring  
28 in current bulk silicon semiconductor processes are few in  
29 number and are localized (i.e., the defects only affect one  
30 or two ICLUs at any particular defect site), and of the fine  
31 grain ICLU structure. The fine grain level of testing  
32 minimizes the area necessary for redundant ICLUs and the  
33 complexity of the placement and routing changes that must be  
34 effected to correct for defective ICLUs. Wafer or large ICs  
35 that indicate larger than normal numbers of defects or  
36 defects that are large in affected area when tested by  
37 testing equipment will cause the wafer to be rejected as  
38 outside of the acceptable bulk manufacturing standards which

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1 are typical of all existing IC lines. The number of defects  
2 to be expected with standard available silicon wafers is  
3 approximately five per  $\text{cm}^2$  currently. This means that  
4 approximately five or less ICLUs can be expected to be  
5 defective per  $\text{cm}^2$ . The number of defects per  $\text{cm}^2$  increase  
6 as device feature sizes decrease, but not dramatically, as  
7 indicated by the current industrial use of 0.8 micron  
8 geometries for 4 Megabit memory devices, which will soon be  
9 in limited production.

10 This rip-up router software process approach takes  
11 advantage of this wafer ICLU defect density characteristic  
12 by employing a CAD rip-up router. This CAD software tool  
13 has only become available recently and heretofore was only  
14 used during the design phase of a large IC in an effort to  
15 conserve designer and computer time. The rip-up router  
16 attempts to make local changes to existing IC metallization  
17 layout and, therefore, avoiding the expense of recomputing  
18 the complete IC's metallization trace routing. The rip-up  
19 router is an automatic tool; it accepts change commands to  
20 the ICLU placement net-list and then computes changes to the  
21 IC's metallization database. This modified IC metallization  
22 database is then processed for input to the E-beam  
23 lithographic equipment; this processing software is the  
24 standard software used to drive the E-beam equipment. The  
25 computer processing time required to do local rip-up route  
26 changes has been measured and found to be typically 1 to 2  
27 seconds on an inexpensive 32-bit minicomputer.

28 The modified net list is next used to produce the  
29 database for the desired interconnect patterns on the wafer  
30 using E-beam means. The metallization process is in one  
31 embodiment a two layer metallization, although a single  
32 layer of metallization or three or more layers of  
33 metallization can also be used. The process involves  
34 depositing a layer of insulation, such as silicon dioxide,  
35 typically of about one micron thickness over the wafer  
36 surface, and cutting vias by means of a mask to the contact  
37 points on the wafer surface through the silicon dioxide  
38 layer. Then a layer of metal, typically aluminum, is

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1 deposited over the silicon dioxide. Then a layer of  
2 photoresist is deposited and patterned, for example using  
3 E-beam (maskless) lithography. The E-beam is controlled by  
4 the CAD database means and its modified net list to make the  
5 desired interconnect pattern corrected in accordance with  
6 the test results. The photoresist is then developed and  
7 removed where not exposed to the E-beam, allowing the  
8 patterning of the interconnects as desired.

9 The metallization process is then repeated for the  
10 second metallization layer and any subsequent metallization  
11 layers. The metallization process is generally well known  
12 technology, the innovation being that the net list is  
13 modified for each die even though the function to be  
14 implemented on each die is identical.

15 At this point the wafer is complete, ready for scribing,  
16 packaging and final test as usual.

17 The tester surface as mentioned above is a key element  
18 of this invention.

19 The tester surface is specially fabricated using  
20 advanced semiconductor manufacturing methods. Starting as  
21 shown in Figure 7 with typically a conventional 5" or 6"  
22 silicon wafer substrate 101 (without any circuitry on it), a  
23 layer of KBr or other release agent 102 is deposited over  
24 the wafer 101 surface, followed by a layer of gold 103 about  
25 1000Å (0.1 micron) thick. Then a layer of silicon dioxide  
26 104 of about one micron thickness is deposited on the wafer  
27 101 surface by means of chemical vapor deposition. This is  
28 a low stress layer, deposited at about 100°F, using  
29 commercially available systems such as provided by Ionic  
30 Systems (Milpitas, CA) or ASM Lithography, Inc. (Tempe,  
31 AZ). The silicon dioxide layer 104 has a surface stress of  
32 about  $10^5$  dynes/cm<sup>2</sup>, making it very flexible. Then, using  
33 conventional mask methods and photoresist layer 106 as  
34 described above, vias such as 108 are etched, down to the  
35 gold layer, in the silicon dioxide layer 104 to define the  
36 probe points. The vias such as 108 are 2 to 4 microns in  
37 diameter.

38 The tester surface, in the preferred embodiment, has two

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1 similar gold metallization layers on top of the wafer. The  
2 first metallization layer is formed by first depositing,  
3 over the KBr layer 102, a silicide layer (not shown) 1000Å  
4 to 2000Å (0.1 to 0.2 microns) thick to act as an etch.  
5 stop. Then the silicide deposition is removed from all but  
6 the vias 108. A nichrome/gold metallization-I layer 112 is  
7 deposited, to a thickness of 1000Å to 2000Å, and a first  
8 layer metal mask and etch are used to define the  
9 interconnect lines by forming traces.

10 Then a second silicon dioxide layer 114, also about one  
11 micron thick, is deposited, followed by the second layer via  
12 116 masking, second layer via etching, nichrome/gold  
13 metallization layer-II 118 and second layer metal mask and  
14 etch as shown in Fig. 9.

15 Next, customized multiplexer circuits such as 120-1 and  
16 120-2 as shown in side view in Fig. 10 are attached to the  
17 metallization-II layer 118. These multiplexers 120-1 and  
18 120-2 are individual die that contact the metallization-II  
19 layer 118 traces as desired, to provide electrical  
20 connections to the tester signal processor. The  
21 multiplexers such as 120-1 and 120-2 are dispersed around  
22 the outer part of the metallization-II layer 118 on the  
23 wafer 101, and serve as programmable input/output means.

24 Next a mechanical structure called a support ring 122,  
25 as shown in top view in Fig. 11, and in side view in Fig.  
26 12, is bonded with epoxy adhesive to the metallization-II  
27 layer 118 on top of the wafer 101. The support ring 122 is  
28 typically a quartz annulus (ring) of the same outer diameter  
29 as the wafer substrate 101 and an inner diameter of 1 to  
30 2 inches.

31 The quartz support ring 122 is in one embodiment  
32 0.1 inch thick. Its inner area 124 is the contact area of  
33 the test surface. The ring 122 thus supports the actual  
34 contact area 124 and provides electrical connections to the  
35 remainder of the test system. The support ring 122 has  
36 holes such as 126-1 and 126-2 (Fig. 11,12) machined into it  
37 to accommodate the multiplexer circuits including 120-1 and  
38 120-2 as shown in Fig. 12.

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1        The support ring 122 and its underlying silicon dioxide  
2 and metal layers are now released from the underlying  
3 silicon wafer 101 shown in Fig. 9. The release agent KBr  
4 (or similar material) was the material first deposited on  
5 the wafer 101. By means of the release agent, scribing  
6 around the edge of the support ring and then dipping the  
7 assembly shown in Fig. 12 in water allows the silicon  
8 dioxide layers to be peeled off the wafer 101. Alter-  
9 natively, without the use of KBr, release can be achieved by  
10 etching the wafer 101 away in an ethylene-diamine  
11 solution.

12        Next, with the tester surface free of the wafer 101, the  
13 first gold deposition layer 103 shown in Fig. 7 is stripped  
14 off, leaving the exposed gold-filled vias such as 108 on the  
15 released surface 130 as shown in Fig. 9.

16        To complete the tester surface, probe points are grown  
17 on the released surface, so that the probe points grow out  
18 from the vias such as 108. To grow the probe points, the  
19 support ring 122 and its attached layers are put in a float  
20 (not shown), and the float placed in an electrolytic  
21 solution containing gold with the exposed ends of the vias  
22 108 as shown in Fig. 9 immersed in the solution. Voltage is  
23 applied and the probe points such as 132 grow by  
24 electrolyzation at the ends of the vias 108.

25        The probe points such as 132 are thus made of gold in  
26 the preferred embodiment and grow out of the central part  
27 124 of the test surface as shown in Fig. 12. The probe  
28 points such as 132 are 2 to 4 microns in diameter, and about  
29 4 microns high. They connect with the metal in each via,  
30 and hence to the two metallization layers. The pattern of  
31 probe points such as 132 on the tester surface is unique,  
32 and corresponds to the contact test points on the wafer to  
33 be tested.

34        Several kinds of probe points 132 can be provided. In  
35 an alternative embodiment, probe point height is determined  
36 by a mask. To provide masked probe points, a mask  
37 containing vias is formed on surface 130 at the probe point  
38 locations, then the points grown in the vias and then the

1 mask removed. The probe points can be aluminum or other  
2 suitable metals or conductive materials.

3 The tester surface itself can be fabricated with  
4 elastomeric probe points such as conductive doped  
5 polyacetylene (personal contact with Professor Alan G.  
6 MacDiarmid, University of Pennsylvania and also see  
7 "Plastics that Conduct Electricity," Scientific American,  
8 Feb., 1988, pgs. 106-111, by Richard B. Kaner and Alan G.  
9 MacDiarmid) that compress on contact with the contact points  
10 of the device or ICLU under test, to allow closer probe  
11 point spacing or to make the tester surface more flexible.  
12 Such elastomeric materials are applied and etched with  
13 established techniques.

14 In a slightly different method to fabricate the tester  
15 surface, the substrate wafer first has etched in its center  
16 a circular depression one to two inches in diameter and  
17 typically twenty mils deep. This depression will impart a  
18 gradual extension to the outer part of the tester surface,  
19 so that the center part of the finished surface will extend  
20 slightly below the surrounding tester surface.

21 A different tester surface is illustrated in Figs. 13-  
22 15. Here the multiplexer circuits and tester logic are  
23 integrated into the tester surface. Fig. 13 shows how, as  
24 before, starting with a standard semiconductor wafer 133,  
25 multiplexer and tester logic circuitry 134 is fabricated on  
26 the surface of wafer 133. Then, as described above, a  
27 depression 135 is etched in the center of wafer 133. The  
28 depression 135 is again one to two inches in diameter and  
29 typically twenty mils deep. Then, as shown in Fig. 14,  
30 several layers of silicon dioxide and metallization 136 are  
31 formed on the wafer over depression 135 and over the logic  
32 sites 134. In this embodiment, the tester probe point array  
33 sites such as 138 may (optionally) be etched into the  
34 surface of the wafer 133 in the depression, to allow  
35 preformation of the probe points by filling the etched probe  
36 point sites 138 with metallization.

37 After the tester surface 136 (Fig. 14) is fully  
38 fabricated on wafer 133, the surface 136 is separated from

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1 wafer 133 as before by selective etching away of wafer  
2 133. (Release agents cannot be used here since part of  
3 wafer 133 including logic sites 134 must remain as part of  
4 tester surface 136). The tester surface 136 is attached to  
5 a support ring 150 before the step of selective etching as  
6 shown in Fig. 15, and used in the same manner as described  
7 above with a fluid well 152 and piezoelectric pressure cell  
8 154 provided.

9 Depending on their shape and material, the probe points  
10 such as 132 in the various embodiments will exhibit  
11 mechanical wear when in use to probe the wafer under test.  
12 When worn below tolerance, the points can be refurbished by  
13 dipping in aqua regia to remove them, and then renewed with  
14 the electrolyzation process as before, to produce a remanu-  
15 factured surface.

16 The above description of embodiments of this invention  
17 is intended to be illustrative and not limiting. For  
18 instance, very large circuits can be produced by testing and  
19 metallizing nine adjacent die 240 to 249 (in a 3 x 3 array)  
20 on a wafer 252 as shown in Fig. 16, and then interconnecting  
21 the nine die to form one super die 254.

22 Alternatively, the invention can be practiced not only  
23 at the transistor level, but at the ICLU level such as a  
24 standard gate or custom gates or memory devices. This  
25 involves fewer contact points, and requires redundancy to be  
26 provided in the form of extra gates or groups of gates to  
27 replace defective ICLOUs. The invention is also not  
28 restricted to gate arrays, and could be practiced on any  
29 kind of integrated circuit (e.g., custom logic or DRAM).  
30

31 If the tester surface probe points are enlarged to sizes  
32 of 2x2 mils to 4x4 mils, the tester surface would have an  
33 additional utility as a functional circuit tester for die-  
34 sorting purposes after the manufacturing of the circuit is  
35 completed. This application would increase pin count  
36 density over the prior art.

37 The tester surface can be fabricated from flexible  
38 materials other than silicon dioxide, such as silicon  
nitride or polymers, so long as the materials physically

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1 support vias and conductive traces.  
2 In another embodiment, the tester interconnections are  
3 formed on the surface of the wafer to be tested.  
4 In this embodiment, instead of fabricating a tester  
5 surface of NxM test points in a grid with an interconnecting  
6 set of metallization layers fabricated in the tester  
7 surface, the interconnection metallization is fabricated on  
8 the surface of the wafer (forming direct metallization  
9 contact to the ICLU contact points) and the probe points are  
10 arranged as a ring around this on-wafer tester interconnect  
11 structure. This process would form the same electrical  
12 connection path to the ICLUs to be tested as in the  
13 previously described embodiments. The advantage here is  
14 that much smaller ICLU or contact points could be accessed,  
15 or alternatively this embodiment allows wider spacing of  
16 tester surface probe points and requires fewer of them, i.e.  
17 only N+M points. This embodiment greatly increases the  
18 potential operable range of the invention with only a small  
19 increase in processing costs for the on-wafer metallization  
20 structure. The on-wafer metallization structure is  
21 temporary. It is fabricated out of a metal such as aluminum  
22 and a separation dielectric layer of resist. Once the on-  
23 wafer interconnect structure has been used to test the ICLUs  
24 or devices by the tester surface, the interconnect structure  
25 is etched from the surface of the wafer by normal wafer  
26 cleaning methods.  
27

28 PROBE POINT STRUCTURE AND FABRICATION

29 In accordance with the invention, the diameter of the  
30 probe points varies from several mils to less than a  
31 micron. The larger probe points are typically used in the  
32 construction of functional IC testers where the electrode  
33 contact or pad size on the IC to be tested is typically 2  
34 mils to 5 mils in diameter. Use of the method in the  
35 construction of a functional IC tester allows 1 mil or less  
36 pad size diameter.  
37

38 The various embodiments of the probe point design  
provide a vertical probe point contact adjustment of

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1 approximately 10% to 40% of the length of the probe point.  
2 This adjustment is provided due to the well-known  
3 flexibility of the low stress silicon dioxide ( $SiO_2$ )  
4 material in the probe point or the elastomeric properties of  
5 various conductive polymers such as polyacetylene,  
6 polythiophene or polypyrrole as examples. Thus these  
7 embodiments of the probe point are flexible structures which  
8 recover to their original shape after being flexed. In one  
9 embodiment of the invention, flexibility of certain probe  
10 points allows the use of such probe points in a tester  
11 surface without the need for fluid back pressure as  
12 described above.

13 The adjustable probe point structure is applicable to  
14 both large probe point applications such as a functional IC  
15 wafer sorter system and for the manufacturing of large scale  
16 integrated circuits as practiced in accordance with the  
17 invention. The adjustable probe points in use can be  
18 located on the tester surface at a very small  
19 center-to-center spacing (e.g., approximately 1.5 times to  
20 twice the diameter of the probe point's largest dimension)  
21 and thereby may contact contact pad sizes on the device to  
22 be tested of the diameter of approximately 0.5 micrometer or  
23 less with center-to-center contact pad separation of 1  $\mu m$  or  
24 less. In other embodiments, the probe points have a  
25 diameter of approximately 0.25 micrometers. The probe point  
26 structure is scalable in accordance with CVD (chemical vapor  
27 deposition) process, electroplating processes, and  
28 lithographic technology limitations, and therefore the  
29 fabrication of probe points as described below with  
30 diameters less than 0.1  $\mu m$  is supported.

31 In use, each probe point engages in a wiping action so  
32 as to engage and electrically contact the contact pads  
33 (electrodes) of the circuit device under test. The wiping  
34 action of the probe point at the contact pad of the device  
35 under test is necessary to achieve ohmic contact when  
36 contact pads are made from metals that form overlying thin  
37 films of native oxides such as aluminum. The wiping action  
38 breaks through the thin film of native oxide overlaying the

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1 contact pad. This wiping action is accomplished through  
2 mechanical vibration of the test fluid which is provided  
3 behind the silicon dioxide supporting membrane. In the  
4 embodiment where the tester surface is without a fluid  
5 providing backpressure, a 5 micron to ten mil thick layer of  
6 a conductive elastomeric polymer, such as conductively doped  
7 polyacetylene, is formed over a piezoelectric material layer  
8 on the side directly opposite the probe points of the tester  
9 surface. The elastomeric material absorbs shear stress  
10 experienced by the tester surface brought about by loading  
11 during contact of the DUT and piezoelectric generated wiping  
12 action. The piezoelectric material is then made to vibrate  
13 by supplying it with an electrical voltage of a desired  
14 frequency, which in turn causes a wiping action of the tip  
15 of the probe point on the surface of the substrate being  
16 tested.

17 In accordance with the invention also, a voltage input  
18 frequency to the piezoelectric material controlling the  
19 probe point pressure is used to cause a wiping action of the  
20 probe point tip. The appropriate voltage frequency results  
21 in vibration of the piezoelectric material which in turn is  
22 transmitted to the probe points through the fluid in the  
23 bladder.

24 An additional layer of piezoelectric material, adjacent  
25 to the first layer but separated from the first layer by  
26 approximately 50 mils is used to measure the applied force  
27 on the tester surface. This optional piezoelectric layer  
28 generates a small voltage when mechanical stresses are  
29 applied to it. These voltages are read and converted to  
30 load equivalent measurements on the tester's surface. These  
31 measurements are used to determine an over-load pressure on  
32 the tester surfaces as shown in cross-section view of tester  
33 surface and support plate, Figure 17(a). Figure 17(a) shows  
34 in cross-section the tester surface membrane 270 and support  
35 plate 272 with the use of a piezoelectric material 274 as a  
36 pressure sensor in the fluid-filled bladder 276 of the  
37 tester surface. The fluid port 278 and piezoelectric  
38 generator 280 are also shown.

1        The physical placement orientation of the tester may be  
2 below (i.e., underneath) the DUT substrate. This would  
3 prevent any downward distortion of tester surface  
4 membrane 270 from the fluid 276 behind the membrane 270 due  
5 to gravity. Instead the positions of tester surface 270 and  
6 the DUT substrate (not shown) are in reverse order from what  
7 one would intuitively expect, or the DUT substrate is held  
8 over tester surface 270 and tester surface 270 is raised to  
9 make contact with the DUT. In this manner it is easier for  
10 tester surface 270 to maintain its originally formed shape  
11 while under internal fluid pressure. Incremental mechanical  
12 vertical adjustment means will be sufficient in many  
13 applications to bring all the probe points (not shown) of  
14 the tester surface into full contact with the DUT without  
15 resorting to the application of additional piezoelectric  
16 generated pressure from pressure generator 280.

17        Probe Point Structure

18        The following describes two kinds of probe point  
19 structures and various probe point tip designs in accordance  
20 with the invention. These probe point structures and tip  
21 designs can be used in unrestricted combination on a Tester  
22 Surface.

23        Solid probe point.

24        As seen in Figure 17(b), in one embodiment a solid probe  
25 point, which bends (flexes) horizontally to adjust to  
26 vertical contact loading, is relatively thin and elongated  
27 with a length to diameter ratio of approximately 1-10 to  
28 1-40. Figure 17(b) shows in cross-section a solid probe  
29 point structure with a central electrode 282 formed by CVD  
30 tungsten. Central electrode 282 provides contact between  
31 the metal probe point tip (preferably titanium or tungsten  
32 plated with gold) 284 and an interconnect trace in tester  
33 surface 286. The shaft 288 of the probe point is low stress  
34 CVD silicon dioxide, as is tester surface membrane 290.  
35 Together, silicon dioxide layers 288, 290 form tester  
36 surface 292.

37        As seen in another embodiment in Figure 18, the probe  
38 point 312 has a silicon dioxide core 314 with a thin metal

1 cylinder 316 formed around core 314, and an external layer  
2 318 of silicon dioxide. Also provided are metal tip 320,  
3 metal trace electrode 322, and flexible  $\text{SiO}_2$  layers 324,  
4 326. Layers 318, 324, 326 together form tester surface  
5 328. Cylindrical electrode 316 provides greater current  
6 carrying surface area than does the solid central electrode  
7 of Figure 17b.

8 Compressible Probe Point.

9 A second probe point structure 330, which is  
10 compressible, is shown in Figure 19a. Probe point 330 is  
11 hollow and uses a fluid back pressure acting against the  
12 interior 332 of the probe point 330 to cause the  
13 compressible probe point 330 to recover its original shape  
14 after a load 334 (i.e., an IC contact point 336) which is  
15 compressing the probe point 330 has been removed. Probe  
16 point 330 includes a tip 338 of tungsten or titanium plated  
17 with gold, a wall 340 of silicon dioxide which is 100 $\text{\AA}$  to  
18 4000 $\text{\AA}$  thick, and an inner gold electrode 342 of tungsten or  
19 titanium 10 $\text{\AA}$  to 1000 $\text{\AA}$  thick plated with gold. Also shown is  
20 tester surface 344, which is 1.5 to 4.0  $\mu\text{m}$  thick. Probe  
21 point 330 is shown in its compressed (i.e. "imploded")  
22 configuration under load 334 in Figure 19(b).

23 As shown in Figure 20(a), another probe point structure  
24 348 has a diameter  $d$  of approximately 1 to 4 micrometers and  
25 a height  $h$  of approximately 4 to 12 micrometers. The wall  
26 of probe point 348 is composed of a layer of silicon dioxide  
27 350, and an embedded layer of metal 352, with a total thick-  
28 ness of approximately 100 $\text{\AA}$  to 4000 $\text{\AA}$ . The tester surface 354  
29 is silicon dioxide, typically 1.5 to 4.0  $\mu\text{m}$  thick. The wall  
30 of the probe point may also be composed of a layer of metal  
31 and an internal layer of silicon dioxide with a similar  
32 probe point 348 wall thicknesses in cross-section. The  
33 interior 356 of the probe point is hollow to allow a fluid  
34 to enter and fill the interior 356. The tip 358 of the  
35 probe point is preferably a refractory metal with gold such  
36 as tungsten/gold or titanium/gold as  $d$  scribed b low.

37 Prob point 348 of Figure 20(a) is shown in Figure 20(b)  
38 wherein probe point 348 is compressed by contact with a

1 contact pad 362 of a circuit device under test 360. As  
2 shown in Figure 20(b), the probe point height is compressed  
3 by approximately 1 to 4 micrometers. The sidewalls 350, 352  
4 of probe point 348 partially collapse due to the non-elastic  
5 nature of the silicon dioxide layer 350. However, the  
6 relative thinness of the sidewalls 350, 352 of probe point  
7 348 and their low surface tension allow the probe point 348  
8 to recover its shape when the load is removed as in Figure  
9 20(a). The fluid filling the interior portion 356 of probe  
10 point 348 is preferably commercially available Florinert.  
11 The sidewalls 350, 352 of probe point 348 are substantially  
12 thinner than the supporting low stress silicon dioxide  
13 membrane 354, which has a thickness of typically 1.5 to 4  
14 micrometers. The sidewall of the probe point 348 includes  
15 an embedded metal cylinder electrode 352 which connects the  
16 metal probe point tip 358 with electrically conductive  
17 interconnect structures (not shown) interior to the silicon  
18 dioxide membrane 354 supporting probe point 348.

19 Optionally, in the case of compressible probe point 348,  
20 during fabrication (described below) the interior of the  
21 probe point 356 may be filled by metal deposition and  
22 selectively etched removed until only the metal at the  
23 interior tip 358 remains. This metal backing of the probe  
24 point tip 358 strengthens it.

25 Hybrid Probe Point Structure

26 Figure 21 shows in cross-section a hybrid (both solid  
27 and compressible) probe point structure design. This  
28 structure provides stress minimization where the probe point  
29 attaches to the tester surface 363. The probe point is  
30 preferably fabricated primarily from low stress silicon  
31 dioxide 364-1, 364-3, 364-4. The probe point has a metal  
32 (preferably CVD tungsten) core 364-2 with external silicon  
33 dioxide walls 364-1. Also shown is titanium or tungsten  
34 gold plated tip 365, and metal trace layer 364-5.

35 Other Probe Point Structures

36 Figure 22 shows in cross-section three compressive-type  
37 probe points 366-1, 366-2, 366-3 with respectively blunt  
38 metal probe tips 368-1, 368-2, 368-3 on the tester surface

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1 370. Tester surface interconnect trace 372 is shown making  
2 contact with the cylinder shaped electrode 374 of a probe  
3 point such as 366-2 embedded in the low stress silicon  
4 dioxide tester surface 376 and side wall of probe point  
5 366-2 and providing a connection between the tester surface  
6 interconnect trace 372 and probe point tip 368-2. An  
7 optional hard metal backing interior to the probe point and  
8 just behind probe point tip 368-2 is not shown.

9 Each probe point 366-1, 366-2, 366-3 has a similar  
10 diameter  $d$  and is compressible with a center-to-center  
11 spacing  $x$  between adjacent probe points. Distance  $x$  is  
12 typically 1 to 20 microns; but is preferably a distance of  
13 no less than approximately 1.5 times distance  $d$ . This  
14 spacing allows the tester surface to probe integrated  
15 circuits of minimum feature sizes at the device (i.e.  
16 transistor) level. Figure 22 shows probe points 366-1,  
17 366-2, 366-3 in an unloaded configuration.

18 Figure 23 shows in cross-section the same probe points  
19 366-1, 366-2, 366-3 of Figure 22 in contact (under load)  
20 with a DUT 380. The figure shows that the compressible  
21 probe points 366-1, 366-2, 366-3 each accommodate the height  
22 variances of the various DUT contacts 380-1, 380-2, 380-3,  
23 thus showing the independent height adjustment capability of  
24 each probe point which can be as much as 40% of its  
25 length. As shown, each probe point 366-1, 366-2, 366-3  
26 (exclusive of metal probe point tip 368-1, 368-2, 368-3)  
27 deforms approximately 1 micrometer for every 2 to 3  
28 micrometers of probe point height. The surface thickness of  
29 the probe point wall 382 is approximately one quarter or  
30 less of the thickness of the supporting test structure  
31 membrane 370. In the case of functional tester application  
32 where probe points may approach or exceed one mil diameter,  
33 the probe point wall (or sidewall) may be the same thickness  
34 as the supporting test structure membrane. A thinner wall  
35 of the probe point will result in greater flexibility.

36 Figure 24 shows another configuration of compressible  
37 probe points 386-1, 386-2, 386-3 with a pointed probe point  
38 tip 388-1, 388-2, 388-3. The shape of each probe point tip

1 such as 388-1 contributes to the contact capability of the  
2 probe point 386-1 independently of the diameter of the probe  
3 point body 390 by providing a smaller probe point contact  
4 feature size and improving the efficiency for breaking  
5 through native metal oxides that may form on a contact pad  
6 to be probed. Various probe point tip designs can be  
7 fashioned by the probe point fabrication process in  
8 accordance with the invention as described below.

9 As shown, the center-to-center x spacing between the  
10 probe points is approximately 3 to 6 micrometers. Each  
11 probe point is approximately 2 to 4 micrometers in diameter  
12 d. The height h of each probe point is approximately 4 to  
13 10 micrometers. As shown in Figure 25, the same structure  
14 shown in Figure 24 when under load from DUT 392 is deformed  
15 slightly. The side wall, which is approximately 1000Å to  
16 4000Å  $\mu$ m thick, is compressed by the load of DUT contacts  
17 394-1, 394-2, 394-3. The tester surface 396 is  
18 approximately 1.5 to 4 micrometers in thickness.

19 Tester surface 396 is preferably low stress silicon  
20 dioxide or silicon nitride. Each probe point tip 388-1,  
21 388-2, 388-3 is constructed of a hard core such as titanium  
22 or tungsten (an appropriate barrier metal layer may be used  
23 to prevent the formation of native oxide on the selected  
24 hard metal) which is optionally electroplated with pure  
25 gold. The pointed probe point tips 388-1, 388-2, 388-3 of  
26 the probe point in this embodiment allows low pressure  
27 contact to be made to the device under test 392. The  
28 compressible probe point structure allows uniform pressure  
29 for all probe points and to provide independent vertical  
30 adjustment of closely spaced probe points 386-1, 386-2,  
31 386-3.

32 Figures 26(a) and 26(b) show another configuration of  
33 hybrid probe points with a compressible probe point body  
34 portion 400 supporting an elongated solid probe point 402.  
35 The compressible portion 400 of the probe point as described  
36 above is hollow and typically filled with a fluid 404. As  
37 shown in Figure 26(b), the probe point configuration of  
38 Figure 26(a) is compressed under a load 406. The solid

1 portion 402 of the probe point has a diameter  $s$  of  
2 approximately 0.5 to 1.0 micrometers. The side walls of the  
3 compressible probe point portion 400 are approximately  
4 0.25-.5 micrometers thick and formed of low stress silicon  
5 dioxide 408 with internal metal 410. The compressible  
6 portion 400 of the probe point has a diameter  $d$  of  
7 approximately 1-5 micrometers.

8 The probe point compressible portion 400 is formed on a  
9 tester surface 412 which is typically 1.5 to 4.0  $\mu\text{m}$  thick.  
10 The tip 414 of the solid portion 402 is tungsten or titanium  
11 plated with gold.

12 Probe Point Fabrication.

13 In the above-described probe point structures, the probe  
14 point preferably has a hard metal tip in order to electri-  
15 cally contact the contact electrodes or pads of the device  
16 under test. The tip can have various shapes such as a  
17 flattened cone as shown in Figures 22 and 20(a), or pointed  
18 as shown in Figures 19(a) and 24. The probe point tip as  
19 described above preferably has a hard metal core such as  
20 tungsten or titanium, and a gold plated surface which can be  
21 periodically replated as a maintenance step. These probe  
22 point structures are dimensionally scalable in accordance  
23 with conventional semiconductor process technologies, and  
24 with the decreasing circuit device element minimum feature  
25 sizes, to allow electrical contact with various circuit  
26 device contact pads (electrodes) of  $1\mu\text{m}$  or less diameter.  
27 The fabrication of the probe points is accomplished as  
28 follows to produce a probe point of approximately one-half  
29 to several micrometers in diameter. Figures 27(a) through  
30 27(h) show fabrication of a compressible probe point;  
31 Figures 28(a) through 28(h) show corresponding steps in the  
32 fabrication of a solid probe point as described immediately  
33 below.

34 1. Trench or etch a hole 420 (Figures 27(a) and 28(a))  
35 with a depth and diameter equal to the dimensions of the  
36 desired probe point body in the semiconductor substrat 422  
37 (wafer) or substrate material upon which the test r surfac  
38 will subsequently be deposited. Optionally, a 0.5 to 2  $\mu\text{m}$

1 layer of low stress silicon dioxide (not shown) may be  
2 applied prior to etching providing an initial tester surface  
3 thickness. Deposit by CVD (Chemical Vapor Deposition) means  
4 a 100Å to 2000Å thickness of low stress silicon dioxide 424  
5 in the trench or hole 420 as in Figures 27(b) and 28(b). In  
6 one embodiment, one first deposits a very thin (100 Å)  
7 barrier (protective) layer such as nichrome or tungsten (not  
8 shown) to separate the probe point from the substrate 422  
9 during selective etch removal of the substrate; the  
10 protective metal later is subsequently removed.

11 2. CVD 100 Å to 300 Å of tungsten 426 and optionally,  
12 a metallization enhancement deposition of 200 to 1000 Å of  
13 gold over the low stress silicon dioxide layer 424, as in  
14 Figures 27(c), 28(c). Mask and fashion metal traces in the  
15 tungsten layer 426 between probe point trenches 420 on the  
16 substrate 422 surface with conventional techniques as  
17 required.

18 3. CVD low stress silicon dioxide 428 from 1000 Å to  
19 2000 Å thick into the trench 420, completely (or nearly so)  
20 filling the trench 420 which is the case in fabricating the  
21 solid probe structure in Figure 28(d). In the case of  
22 compressible probe structures in Figure 27(d) it may be  
23 desired to subsequently fill the trench 420 with a poly-  
24 silicon or metal layer 429 and then by selective etch remove  
25 the deposited material except for the last 1 or 2 µm in  
26 order to form a hardened backing to the probe point tip that  
27 is interior to the probe point.

28 4. Open vias 432 to probe points and deposit one or  
29 more additional metallization interconnect layer 434 as  
30 shown in Figures 27(d), 28(d) with a dielectric layer 436,  
31 438 of low stress silicon dioxide of appropriate thickness  
32 to achieve the overall desired silicon dioxide thickness of  
33 the tester surface.

34 5. After the tester surface has been bonded to the  
35 support plate (not shown), probe point tip processing is as  
36 follows:

37 (a) Selectively etch substrate 422 until 1 to 2 µm  
38 of the tip 440 of the probe point structures is exposed as

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1 in Figures 27(e) and 28(e).

2 (b) Etch any barrier metal layer and first layer  
3 of low stress silicon dioxide 424 to expose the first metal  
4 layer 426 in Figures 27(f) and 28(f).

5 (c) Electroplate refractory or hard metal 442 by  
6 applying the appropriate uniform voltage potential to the  
7 exposed probe electrodes 426 and by placing the tester head  
8 assembly in a float so that only the tester surface is  
9 submerged in the electroplating bath (not shown). Or  
10 alternatively in combination with standard IC resist  
11 patterning techniques as in Figures 27(g) and 28(g), pattern  
12 with resist mask 446 and etch to form a mold for the probe  
13 tips as desired with conventional IC processing. Probe tip  
14 hard metal thickness may vary from 1000 Å to several µm.

15 Figures 27(g), 28(g) also show the use of two layers of  
16 resist. The first layer of resist 446 (i.e., first  
17 deposited on substrate 422) is developed through an opening  
18 448 in a second resist layer 450. The harder protective  
19 second resist layer 450 allows the sidewall of opening 450  
20 through the first resist layer 446 to be etched with an  
21 undercut forming a mold for the probe point tip 442. The  
22 use of two resist layers 446, 450 to form an opening 450  
23 with an under-cut sidewall as shown is conventional IC  
24 processing.

25 (d) Complete the selective etch removal of  
26 substrate 422 and any metal protection barrier as in Figures  
27 27(h) and 28(h).

28 (e) Electroplate the probe point tip with a gold  
29 layer 454 (.9999 pure) to promote ohmic contact to the DUT  
30 (not shown), or electroplate with other metal such as  
31 copper; the electroplating is achieved by applying a uniform  
32 voltage potential to all or selected portions of the probe  
33 points. The voltage potential is supplied to the probe  
34 points through the metal interconnect traces 426, 434 that  
35 have been fabricated in the tester surface.

36 As described above, the probe point tip fabrication  
37 process involves selectively etching away the substrate in  
38 which the probe point is formed, first exposing an

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1 appropriate portion of the tip of the probe point. The  
2 selective etching of the substrate is then stopped (the  
3 substrate acting effectively as a protective layer for the  
4 lower portion of the probe point protecting the external  
5 silicon dioxide layer of the tester surface), and the  
6 exposed silicon dioxide layer of the probe point tip is  
7 etched away to expose the metal core of cylindrical  
8 electrode, and then the probe point is plated up or enhanced  
9 with a refractory metal such as tungsten or titanium. The  
10 selective etch of the remaining portion of the substrate to  
11 be removed is then continued.

12 In an alternate embodiment (see Figure 29) of probe  
13 point fabrication, the probe point tip is fabricated first  
14 by patterning a thin film of metal deposition 460 on a  
15 silicon substrate, and then covered with polysilicon or a  
16 polymer layer 462 of 4 to 10  $\mu\text{m}$  thickness through which  
17 holes such as 464 are anisotropically etched to the pre-  
18 formed probe point tips in which the probe points are formed  
19 (as also shown in Figures 27(a), 27(c) and 27(d)) as shown  
20 in cross-section in Figure 29. Also shown in Figure 29 are  
21 as described above tungsten/gold layer 468, and low stress  
22 silicon dioxide layers 470, 472, 474 and electrode 476.

23 Once the probe points are fabricated the silicon  
24 substrate 466 and the polysilicon or polymer layer 462 are  
25 selectively etched away leaving free standing probe points  
26 as shown by Figures 27(h) or 28(h). This alternate  
27 fabrication method allows the probe point tips to be  
28 fabricated first, therefore avoiding fabrication steps while  
29 selectively etching the substrate away from the probe  
30 points. This embodiment is most effective for probe points  
31 of less than 10  $\mu\text{m}$  in length.

32 Probe Point Tester Surface Interconnect Structure

33 The following describes preferred embodiments of the  
34 interconnect metallization in the tester surface which  
35 connect the probe points to integrated circuitry on the  
36 tester surface about the probe point bladder area, or to  
37 contact pads about the probe point bladder area. The method  
38 and structure described here provides the simultaneous

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1 access to a plurality of ICLUs or circuit devices for the  
2 purpose of testing them with a generic row and column  
3 organization method, and requiring typically only two layers  
4 of interconnect metallization in the tester surface. The  
5 organization of the interconnect metallization and the  
6 control logic it connects to are independent of the  
7 placement of the ICLUs on the surface of the substrate to be  
8 tested. Only the positioning of the probe points and the  
9 test signal are specific to the ICLUs of the DUT.  
10 Therefore, the design of each tester surface does not  
11 require a custom layout/logic design to fit the placement of  
12 ICLUs of the DUT.

13 Figure 30 shows a top view of a tester surface. Shown  
14 are x-axis probe point interconnect traces 480-1, 480-2,  
15 ..., 480-k which together are one metallization layer and y-  
16 axis probe point interconnect traces 482-1, 482-2, ...,  
17 482-k which are a second metallization layer. The x-axis  
18 traces 480-1, 480-2, ..., 480-k are connected to integrated  
19 row (x-axis) selection control logic and test signal  
20 generator circuitry 484 mounted on tester support plate  
21 486. The y-axis traces 482-1, 482-2, ..., 482-k are  
22 connected to integrated column (y-axis) selection control  
23 logic and test signal receivers circuitry 488, also mounted  
24 on tester support plate 486. The edge 490 of tester fluid  
25 bladder 492 defines the effective test surface area.

26 The interconnect metal layers are designed to provide  
27 simultaneous contact to all of the ICLUs or circuit devices  
28 for a specific area of the DUT in one physical contact, and  
29 provide the ability to test the ICLUs in a sequential or  
30 parallel fashion. The fine-grain approach in accordance  
31 with the invention requires only a limited number of probe  
32 points to test an ICLU. Therefore, for each small area of  
33 substrate in which the ICLU is fabricated, a number of probe  
34 points must be provided. The probe points required per ICLU  
35 or circuit device will typically vary from two to ten. The  
36 placement of the ICLUs may be orderly as in the case of a  
37 gate array or memory circuits, or random as in the case of a  
38 custom circuit design, but the organization of the

1 interconnect to the probe points for the ICLUs to be tested  
2 are approximately a row and column structure from a testing  
3 procedural stand-point.

4 The interconnect metallization structure of the tester  
5 surface will typically have two layers of metallization as  
6 shown in Figure 30, but three and four metal layers of  
7 designs are used in other embodiments. All the traces of a  
8 specific metal layer are patterned parallel to either one of  
9 two reference layout coordinate axes (the x-axis or y-axis)  
10 as shown in Figure 30.

11 ICLU input signal and/or power voltage reference are  
12 provided along one axis (x-axis), and ICLU output signal  
13 and/or ground voltage reference are provided along the  
14 orthogonal axis (y-axis). In this manner by selecting  
15 (addressing) specific metal traces by control logic on  
16 either axis, a specific ICLU can be independently tested at  
17 the intersection of the metal traces.

18 The information for the selection and test signal  
19 generation on an ICLU specific test basis is derived from  
20 the CAD layout database of the circuit. The CAD layout  
21 database defines the placement of ICLUs (input and output  
22 electrode contacts) and the circuit function (electrical  
23 specification) of the ICLU. This provides the information  
24 sufficient for placement of tester surface probe points and  
25 metal trace interconnection identification for subsequent  
26 selection of the ICLU during testing.

27 An ICLU is tested when x-axis and y-axis metal traces  
28 are selected specific to the one ICLU that is at the  
29 intersection of the selected x-axis (row) and y-axis  
30 (column) metal traces. Therefore, during one physical  
31 contact with the DUT by the tester surface, all the ICLUs of  
32 interest in probe point contact with the tester surface are  
33 simultaneously tested in an electronic sequential row versus  
34 column selection process. Input and output signals are  
35 organized by reference axis to prevent the testing of an  
36 ICLU other than the ICLU of interest.

38 ICLUs are electronically tested in parallel when  
multiple column (output) metal traces corresponding to the

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1 output signals of two or more ICLUs are selected by separate  
2 signal processing test control electronics versus the  
3 selection of one row (input) of metal traces which provide  
4 common input signals to all the ICLUs of interest in the  
5 selected row. This requires that the ICLUs or circuit  
6 devices undergoing parallel testing in this manner have  
7 identical input function, i.e. the selected ICLUs accept the  
8 same input signals, but may generate the same or varying  
9 output signals within the definition of the test being  
10 performed. Therefore, during one physical contact with the  
11 DUT by the tester surface, all the ICLUs of interest in  
12 probe contact with the tester surface are simultaneously  
13 electronically tested in parallel in groups of two or more,  
14 until all the ICLUs of interest have been tested.

15       Figure 31 shows a top view of a tester surface  
16 interconnect metallization similar to that in Figure 30  
17 except the device of Figure 31 is partitioned into four  
18 equivalent areas 496-1, 496-2, 496-3, 496-4 which can be  
19 operated independently of each other (i.e. in parallel).  
20 This allows for higher tester throughput, and the  
21 simultaneous testing of functionally different ICLUs. It  
22 should be noted that similar independent parallel testing  
23 capability can also be achieved by using more layers of  
24 interconnect metallization, where each two layers of  
25 interconnect represent an independent testing means. Shown  
26 are four x-axis integrated selector control logic and test  
27 signal generator circuits 484-1, ..., 484-4, and four y-axis  
28 integrated selector control logic and test signal recover  
29 generator circuits 488-1, ..., 488-4.

30       The testing methods described above are facilitated by  
31 testing the ICLUs or circuit devices prior to the  
32 fabrication of metal interconnect between the ICLUs, and  
33 only the row and column or columns connecting the probe  
34 points to the ICLUs of interest are electrically referenced  
35 by the test control logic. The ICLUs or circuit devices  
36 prior to the fabrication of interconnect metallization are  
37 physically isolated on the substrate upon which they were  
38 fabricated, preventing electrical signals generated by

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1 adjoining ICLUs from being exchanged. The rows and columns  
2 of the tester surface not selected to reference an ICLU or  
3 circuit device are allowed to have high impedance, and  
4 therefore, to "float" (i.e., not to have one of the  
5 reference voltage potentials of the tester surface).

6 Numerous metallization interconnect patterns are  
7 possible for the tester surface to provide for increased  
8 parallel testing capability. Alternate methods of  
9 patterning the metallization interconnect may require more  
10 metal layers or partitioning of the pattern, as shown in  
11 Figure 31. The invention is not limited to the examples as  
12 shown in Figures 30 and 31.

13

14 Active-Matrix Probe Point Control

15 An embodiment of the tester surface called "Active-  
16 Matrix" places a switching mechanism such as dual-gate JFET  
17 or MOSFET transistors adjacent each probe point for purposes  
18 of controlling the reference voltage into a probe point  
19 (i.e., input to the DUT) or output voltage from a probe  
20 point. The gates of each transistor are connected to a pair  
21 of orthogonal (x and y-axis) control metal traces from the  
22 control logic which are separate from the metal traces which  
23 supply test signals. This three or four metal layer  
24 interconnect structure significantly improves parallel ICLU  
25 testing capability. The active-matrix probe point structure  
26 is not limited by the use of JFET or MOSFET gates for  
27 controlling the conductive path to each probe point, other  
28 electronic switching devices that can be fabricated between  
29 the probe points may also be used. The Active-Matrix  
30 switch control logic is fabricated adjacent and  
31 interconnected to various or all of the probe points of a  
32 tester surface. The preferred fabrication technique uses  
33 established DI (Dielectric Isolation) substrate fabrication  
34 methods such as ZMR (Zone Melt Recrystallization) or ELO  
35 (Epitaxial Lateral Overgrowth) to fabricate a crystalline  
36 semiconductor substrate in which the control logic is  
37 formed. Figure 32 shows in cross-section a tester surface  
38 498 with control logic 500 embedded in tester surface 498

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1 adjacent each probe point 502. The electrode interconnect  
2 between the probe point tip 504 and the control logic 500,  
3 and the metal traces that connect the switch control logic  
4 500 with the primary tester surface control logic that is  
5 located at the edge of the tester surface are not shown.

6 The switch control logic semiconductor substrate 500 is  
7 fabricated prior to forming the holes in the substrate in  
8 which the probe point structures are formed as described  
9 above. A semiconductor substrate 500 of typically less than  
10 2  $\mu\text{m}$  thick is formed over a patterned layer of dielectric  
11 505 such as silicon dioxide by one of the DI fabrication  
12 methods referenced above, and the desired circuit devices  
13 are formed by standard IC fabrication techniques. In order  
14 to improve the yield of the desired probe point circuit  
15 devices, the circuit devices and redundant devices are  
16 tested in accordance with the invention prior to forming  
17 interconnect metallization, and only functional circuit  
18 devices are used to complete the switch control logic. Once  
19 the switch control logic is fabricated the fabrication of  
20 the tester surface is completed as described elsewhere in  
21 this specification. Figure 32 is not intended to limit the  
22 Active-Matrix embodiment, but is exemplary. The overall  
23 interconnect layout and its control means are regular in  
24 design, or are independent of the placement of individual  
25 ICLUs to be tested on the IC substrate.  
26

27 Application of Polymer and Polysilicon Films in Tester  
28 Surface Fabrication

29 Polymer films have recently become commercially  
30 available at a thickness of less than 10 $\mu\text{m}$ . These films are  
31 mechanically formed and the non-uniformity in thickness of  
32 these films is significant and can vary more than a  
33 micron. Other polymer film utilization issues such as their  
34 ability to be shaped (as required by the bathtub-like  
35 depression in Fig. 15 which can be 2 mils to over 100 mils  
36 deep), low temperature processing restrictions, the  
37 difficulty in the processing of very small vias (typically  
38 with a diameter of less than 10 $\mu\text{m}$ ) sensitivity to standard

1 metal etch chemicals, present limitation to only two metal  
2 layers (one either side of the polymer film, no multiple  
3 metal layers per side), and the attachment or bonding  
4 efficiency of the film with a large number of small metal  
5 traces, limit the effectiveness of present application of  
6 polymer films to probe points of 1 mil diameter and spacing  
7 of approximately 50 $\mu$ m or 2 mils.

8 Low stress silicon dioxide thin films or various other  
9 low stress inorganic thin films made from such materials as  
10 silicon nitride are suitable for the fabrication of the  
11 invention in an implementation capable of testing ICLUs with  
12 contact geometries of less than 4 $\mu$ m and probe point spacing  
13 of less than 8 $\mu$ m. Low stress silicon dioxide is a superior  
14 material over polymers at present for the fabrication of  
15 integrated tester electronics and tester probe surface, and  
16 the forming of independently adjustable probe points.

17 The combined use of conductive elastomeric polymer film  
18 and low stress silicon dioxide or other low stress inorganic  
19 materials may be used to overcome present geometry and metal  
20 layer restrictions that currently limit the use of polymer  
21 films in certain testing applications. Multiple low stress  
22 silicon dioxide and metal layers can be deposited on one or  
23 both sides of a polymer film with the initial layer of low  
24 stress silicon dioxide acting as a protective layer of the  
25 polymer to subsequent metal and via processing steps. This  
26 is directly applicable to the functional testing of ICs in  
27 wafer sort that are currently using membranes of free-  
28 standing polymer film.

29 An alternate embodiment of the flexible tester surface  
30 is the application of conductive elastomeric polymer and a  
31 thin film of metal such as titanium or thin film of low  
32 stress polysilicon or both. The use of these materials  
33 provide a method for adjusting the CTE (Coefficient of  
34 Thermal Expansion) of the tester surface, and a method of  
35 filling the compressible type probe points with a material  
36 other than a fluid to cause the prob point to return to its  
37 original shape after the release of a compressive load.

38 The low stress polysilicon is deposited in the manner

1 formulated by Richard S. Muller, and presented in numerous  
2 publications; one such publication is the IEEE Transactions  
3 on Electron Devices, Vol 35, No. 6, June 1988, "Integrated  
4 Movable Micromechanical Structures for Sensors and  
5 Actuators". The unique preparation of polysilicon taught by  
6 Muller allows the formation of polysilicon free standing  
7 flexible thin films of 1 to 2  $\mu\text{m}$  thickness to be formed, and  
8 in the case of the tester surface preserves its flexible  
9 nature while providing it a CTE that more closely matches  
10 the CTE of the semiconductor substrate upon which the tester  
11 surface is applied.

12 Figure 33 shows the application of this type of  
13 polysilicon 506 in a flexible tester surface. Polysilicon  
14 506 is applied at an elevated temperature between 400° and  
15 650° C and is uniformly applied in the preferred embodiment  
16 directly onto low stress silicon dioxide 507. Polysilicon  
17 506 is patterned with openings into the probe points 508.  
18 The use of polysilicon in the tester surface when the tester  
19 surface is used to test substrates of silicon improves the  
20 registration operating temperature range of the tester  
21 surface probe points in making consistent contact with the  
22 electrodes of the circuit devices to be tested.

23 The conductive elastomeric polymer layer 509 is  
24 deposited onto the tester surface by electroplate  
25 processing. Elastomeric polymer 509 is applied to the  
26 tester surface once it is completed and all top layer  
27 electrodes have been passivated by a dielectric layer such  
28 as low stress silicon dioxide 507 or low stress polysilicon  
29 506. A thin film of conductive metal such as 100Å of  
30 tungsten (not shown) is deposited over the tester surface  
31 and onto the interior vertical walls of the compressible  
32 probe point structures 508. This metal film acts as a  
33 plating electrode for attracting the polymer and its  
34 conductive dopant. A conformal and uniform thin film 509 of  
35 0.5 $\mu\text{m}$  to 4 $\mu\text{m}$  of the conductive elastomeric polymer is  
36 deposited filling the compressible probe points 508. A  
37 subsequent 0.5 $\mu\text{m}$  to 2 $\mu\text{m}$  thin film layer 510 of metal such as  
38 gold, copper or titanium is optionally deposited by

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1 electroplating over polymer layer 509 to passivate the  
2 polymer layer 509, counter balance possible  
3 compression/tension forces in the free standing portion of  
4 the tester surface, and to add additional strength or  
5 durability to the surface as required.

6 The method of depositing the conductive elastomeric  
7 polymer is taught by MacDiarmid of the University of  
8 Pennsylvania as described above. There are numerous  
9 polymers that may be used to form the desired conductive  
10 elastomeric polymer layer, described by MacDiarmid, such as  
11 polyacetylene, polyparaphenylenes, polypyrrole, polythiophene  
12 and polyaniline. The use of a specific polymer is  
13 determined by the acceptability of its fabrication and  
14 operating characteristics.

15

16 Automatic CAD Probe Point Placement Generation From Circuit  
17 Database

18 Also in accordance with the invention, Computer Aided  
19 Design (CAD) automatically generates the probe point  
20 fabrication masks from the device layout placement data in  
21 the database of the IC to be tested. The CAD database of  
22 the IC design contains the placement dimension data for the  
23 electrode contacts of device elements comprising the  
24 integrated circuit to be tested. This placement data  
25 indicates where probe points are to be placed on the  
26 corresponding tester surface membrane. The database also  
27 contains connection data such as source, drain and gate  
28 electrodes, or emitter, collector and base electrodes and  
29 ICLU electrical specification data (e.g., dual-gate  
30 transistor, diode, P-type transistor, etc.). This ICLU  
31 electrode specification data is used by automatic computer  
32 generation means to create probe point placement and routing  
33 patterns from input or output tester logic devices to the  
34 appropriate probe points. The ICLU electrical specification  
35 data is used to generate the control sequence for the  
36 testing of ICLUs and the automated selection of test vectors  
37 appropriate to the electrical function specification of the  
38 ICLU.

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1

2 TESTER HEAD ASSEMBLY STRUCTURE

3 The following describes several embodiments of tester  
4 head assemblies. The two tester head assemblies of Figures  
5 34 and 35 both are immersion liquid-cooled and provide for  
6 one or more wafers of tester logic to have pin connections  
7 directly to the tester surface, and provide the ability to  
8 optionally include tester logic integrated with the tester  
9 surface. Tester assemblies that do not have integrated test  
10 logic would have slower performance due to probe  
11 interconnect length to the DUT (Device Under Test) and hence  
12 signal delay.

13 The tester head assemblies include an interconnect  
14 structure that can use conventional IC technology or  
15 alternatively ICs made in accordance with the invention and  
16 still achieve a high pin count connection to the tester  
17 surface and DUT with a short trace length from tester logic  
18 to DUT of several mm to several cm; the analog/logic/memory  
19 IC package 512 shown in the immersion chamber 514 of the  
20 tester head assembly in Figure 34 is a packaged integrated  
21 circuit assembly, and there can be more than one such  
22 analog/logic/memory unit in the immersion chamber 514. A  
23 tester head assembly incorporating tester surface 516 with  
24 or without integrated control logic 518 on tester surface  
25 516 is provided, tester surface 516 is interconnected to  
26 analog/logic/memory circuit assembly 512 and use is made of  
27 immersion cooling in chamber 514. Use is made of either a  
28 conductive elastomeric contact 520 on the back side of the  
29 tester support plate 522 and between analog/logic/memory  
30 assemblies 512 or of compressible mechanical metal contacts  
31 presently available such as Pogo Contact pins manufactured  
32 by Augat of Attleboro, MA. This provides a probe surface  
33 for functional IC testing with a lower number of probe  
34 points (e.g., less than 2,000) and probe point diameters of  
35 1 to 4 mils, or for fine-grain testing in accordance with  
36 the invention (e.g., more than 2000 probe points with  
37 diameters of less than one mil). Tester surface support  
38 plate 522 with tester surface 516 is preferably detachable

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1 from the immersion cooled analog/logic/memory assembly  
2 enclosure 526. Thus detachable support plate 522 with  
3 tester surface 516 may optionally be made more cheaply than  
4 such a structure which includes fully integrated logic  
5 circuitry 518.

6 The tester surface assembly may be provided with or  
7 without integrated test logic 518. Also provided is a  
8 method of packaging (interconnecting) several wafers of  
9 tester analog/logic/memory in a single cooled compact test  
10 enclosure 526, which for test instrumentation applications  
11 allows short signal length delay to the DUT. The pin  
12 interconnect 528 in the tester head assembly is preferably  
13 made from elastomeric polymer material such as conductively  
14 doped polyacetylene (as disclosed by Prof. MacDiarmid of the  
15 University of Pennsylvania and described above).

16 The cooled analog/logic/memory circuit packaging 512 and  
17 enclosure 526 are actively cooled with a pumped fluid such  
18 as florinert which enters and leaves the enclosure circuitry  
19 through numerous circulation ports such as port 530. The  
20 circuit package assembly 512 can also be passively cooled by  
21 heat conduction through the metal of the enclosure 526, and  
22 optionally through non-pumped fluid filling the enclosure;  
23 this requires significant areas of contact 529 between the  
24 analog/logic/memory circuit package 512 and the enclosure  
25 housing 526 (which acts as a heat sink or heat exchanger  
26 with the external ambient environment) as shown in Figures  
27 34 and 35.

28 The cooled analog/logic/memory circuit packaging 512 and  
29 enclosure 526 as described here in application with the  
30 tester surface of the invention is not intended to be  
31 limited to this application. The packaging and enclosure  
32 can be used as a general purpose electronic packaging and  
33 enclosure, typically for but not limited to ICs manufactured  
34 in accordance with the invention.

35 The embodiment of the tester head assembly as shown in  
36 Figure 34 is a circular assembly shown in cross section  
37 around the centerline C. The assembly is preferably about  
38 six to ten inches (15 to 25 cm) in diameter. The upper end

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1 plate 532 of enclosure 526 provides physical pressure  
2 contact to press the circuit assembly pin contacts 528 into  
3 contact with the contacts of the bottom end plate 524. A  
4 gasket 534 seals the contact surfaces of the upper end plate  
5 532 and the enclosure 526. Suitable connectors (such as  
6 bolts 536, 538) are provided to hold the assembly  
7 together. The piezoelectric or other pressure control is  
8 not shown for simplicity.

9 The design of the enclosure provides for the optional  
10 use of integrated tester surface logic and a dense pin  
11 contact array mechanical interconnection structure that  
12 minimizes the distance between the probe points and the  
13 analog/logic/memory circuitry; the pin contact array can  
14 have in excess of 4,000 pin contacts. The design uses large  
15 ICs fabricated in accordance with the invention, although  
16 PCB (printed circuit board) circuit assemblies can also be  
17 used.

18 A second embodiment of the tester head assembly is shown  
19 in Figure 35; this embodiment is similar to that shown in  
20 Figure 34, except for the omission of the enclosure bottom  
21 plate 524 which leaves the enclosure assembly cavity of  
22 Figure 35 open to direct contact with the tester surface  
23 516. The tester surface support plate 522 when brought into  
24 contact with the enclosure 526 mechanically closes off the  
25 bottom of the enclosure. Figure 35 thus shows a structure  
26 identical to that of Figure 34 except the bottom of the  
27 enclosure 526 is open. The tester surface support plate 522  
28 is used at the closing bottom plate. A gasket (not shown)  
29 forms a liquid tight seal, and the support (bottom) plate  
30 522 is secured by bolts 540.

31 In other embodiments, the portion of the tester surface  
32 which is applied over the DUT is not a free standing  
33 membrane as described above, but is backed by an elastomeric  
34 polymer material or a rigid material such as p lysilicon.  
35 These embodiments of the tester assembly have primary  
36 application in the functional testing of ICs where probe  
37 point diameters are typically greater than 10 $\mu$ m and are  
38 fabricated in combination with conductive elastomeric

1 polymer materials, or in fine-grain testing applications  
2 where planarity of the DUT is sufficiently flat to allow  
3 probe point contact without excessive pressure  
4 discontinuities across the tester surface that can result in  
5 damage to the tester surface or the DUT, or a shortened  
6 life-time to the tester surface. These embodiments,  
7 however, are not limited to testing applications.

8

9 DISCRETIONARY METALLIZATION INTERCONNECT FOR IC FABRICATION

10 Discretionary metallization interconnect methods for an  
11 IC are provided using the tester in accordance with the  
12 invention and incorporating the use of an optical stepper  
13 and either E-Beam or Ion-Beam equipment. Once the tester  
14 means has determined required changes to a metallization or  
15 via layer of an IC, fine-grain changes are effected with the  
16 use of conventional optical stepper and E-Beam or Ion-Beam  
17 equipment by making modifications to the exposed litho-  
18 graphic pattern after the application of a master fixed mask  
19 pattern. The methods discussed are not restricted to  
20 specific resist materials or techniques, and single or  
21 multi-layered resists are used as required. These fine-  
22 grain discretionary metallization interconnect methods  
23 avoid the requirement that separate and unique exposure  
24 masks be prepared for the patterning of metal or dielectric  
25 thin film layers affected by discretionary interconnect  
26 changes due to defective ICLUs. These novel techniques  
27 result in lower processing costs and a reduction in mask  
28 related manufacturing costs, versus prior art discretionary  
29 techniques.

30 Standard optical negative resist exposure using a fixed  
31 mask is applied, and at this process step a second exposure  
32 by the optical stepper system is performed on the same  
33 undeveloped resist layer. This second step consists of  
34 positioning the lens of the stepper (without a mask) over a  
35 defective area as determined by the tester, adjusting the  
36 opening of the shutter mechanism of the stepper, and making  
37 one or more rectangular exposures that expose completely and  
38 only the area of the resist over the defective area where

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1 discretionary metal or via patterning is to be performed.  
2 Standard resists and etch processing is then resumed. The  
3 result of this augmented optical exposure step is to leave  
4 the area of the metal or dielectric thin film requiring  
5 discretionary patterning unpatterned by the initial exposure  
6 of the fixed mask pattern while patterning the remaining  
7 area, according to the original fixed mask pattern, as would  
8 be expected.

9 Figures 36(a) through 36(d) show in cross-section the  
10 use of negative optical resist and a fixed mask to form a  
11 pattern for etching a thin metal film 560 on a substrate 562  
12 in conjunction with a second optical stepper exposure of an  
13 area requiring discretionary patterning such that the  
14 originally formed pattern of the fixed mask over the  
15 discretionary area is not patterned.

16 An exposed fixed mask pattern in Figure 36(a) on a  
17 negative resist layer 564 requires fine-grain discretionary  
18 changes 566, due to defective ICLUs (not shown) as  
19 determined by the fine-grain tester, below the various  
20 portions of the fixed mask pattern exposure 568. The  
21 unexposed portions of resist are at 570. An optical stepper  
22 without a mask completely exposes in Figure 36(b) the  
23 rectangular areas 572 of the negative resist over the areas  
24 requiring discretionary patterning, such that the original  
25 pattern in these rectangular areas 572 is erased from the  
26 resist 564. The resist 564 is developed and the underlying  
27 thin film 576 etched, in Figure 36(c) and this leaves the  
28 thin film areas 578 requiring discretionary patterning  
29 unpatterned due to the nature of negative resist which is to  
30 develop (remain) where exposed. The resist is stripped in  
31 Figure 36(d) and the remaining unpatterned areas 580 of the  
32 thin film designated by the tester are not patterned to  
33 prevent the interconnection of defective ICLUs. This method  
34 is applicable to both metal and dielectric thin films.

35 The use of a negative resist results in exposed areas of  
36 resist forming the desired pattern after development of the  
37 resist (as indicated by the hatched areas of resist). The  
38 use of negative resist allows the original pattern formed by

1 the initial application of the fixed mask to be "erased" by  
2 a second exposure over areas that contain a circuit defect  
3 as determined by the tester means and where discretionary  
4 patterning (wiring) is required. The remaining unpatterned  
5 discretionary area is subsequently patterned by a second  
6 resist patterning and etch step with either well known  
7 optical means, E-beams, or Ion-Beam exposure.

8 If the choice of a negative photo-resist is inadequate  
9 for the desired optical lithographic resolution of the  
10 process step, an alternative method is to apply first a thin  
11 layer of negative resist over the substrate which is  
12 optically exposed (without a mask and by controlling the  
13 shutter mechanism) only over the areas of the substrate  
14 requiring discretionary patterning. Once developed, the  
15 negative resist will cover only the discretionary areas to  
16 be patterned, preventing these areas from being etched  
17 during subsequent processing. The standard positive photo-  
18 resist is then applied, exposed and developed over the  
19 substrate including the negative resist covered areas. The  
20 layer is etched and the two resist layers are stripped. The  
21 areas requiring discretionary patterning are left  
22 unpatterned.

23 Figures 37(a) through 37(e) show in cross-section the  
24 use of positive optical resist and a fixed mask to form a  
25 pattern for etching a thin metal film 600 on a substrate 602  
26 with the prior application, exposure and development of a  
27 negative optical resist layer 604 over an area requiring  
28 discretionary patterning as determined by the tester. The  
29 negative resist 604 over the discretionary areas prevents  
30 patterning of the metal film 600 by the positive resist and  
31 subsequent etch steps. In Figure 37(a), negative resist  
32 layer 604 is applied over thin metal film layer 600.  
33 Negative resist layer 604 is exposed, by optical stepper  
34 equipment with shutter control and without a mask, at  
35 rectangular areas 606 (in the plane of substrate 602). The  
36 rectangular areas 606 are determined by the fine-grain  
37 tester as overlying defective ICLUs (not shown). Negative  
38 resist layer 604 is developed and the exposed areas such as

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1 area 606 remain.

2 In Figure 37(b) a layer of optical positive resist 610  
3 is applied and patterned by a fixed mask exposure step to  
4 define exposed areas 610-1 and unexposed areas 610-2.  
5 Portions 610-3 of the positive resist layer overlying the  
6 developed negative resist layer 606 do not pattern the thin  
7 film 600 in the steps shown in Figures 37(c) and 37(d).

8 The positive resist layer is developed as shown in  
9 Figure 37(c), leaving a pattern 612 in the positive resist  
10 layer. Then the structure is etched as shown in Figure  
11 37(d); the discretionary area 614 thin film is left  
12 unpatterned, preventing interconnection to the underlying  
13 defective ICLUs. In the next step in Figure 37(e), the  
14 remaining resist layers are stripped, leaving a patterned  
15 thin film with discretionary area 614 unpatterned. The  
16 result is the same as that shown by Figures 36(a) through  
17 36(d), in that the metal film over the discretionary area is  
18 not patterned during the etch processing step, and is  
19 patterned by a subsequent patterning step.

20 Figures 38(a) through 38(e) show in cross-section the  
21 use of positive optical resist to protect an existing metal  
22 film pattern 620 on substrate 622, exposed and developed  
23 over an area requiring discretionary patterning, and the use  
24 of negative E-Beam or Ion-Beam resist applied over the  
25 developed positive resist to pattern a discretionary area.

26 Positive optical resist 624 is applied over a thin film  
27 620 previously patterned by a fixed mask and exposed by  
28 shutter control (maskless) of stepper equipment over the  
29 discretionary areas 626 as pre-determined by the tester  
30 means. When developed, the unpatterned thin film 628 of the  
31 discretionary area is left exposed, and the remaining  
32 patterned portion of film 620 covered (protected from etch  
33 processing) by the developed (unexposed) positive resist  
34 624. A negative E-Beam or Ion-Beam resist 630 is applied in  
35 Figure 38(b) and a discretionary pattern 632 over the  
36 unpattern thin film areas 628 is expos d. The exposed  
37 pattern 634 is developed in Figure 38(c), and th underlying  
38 thin film etched in Figure 38(d), leaving areas 636. Thus,

1 the previously patterned portions of the thin film are  
2 protected from the etch process step by the developed  
3 positive resist 624. The resists are stripped in Figure  
4 38(e) leaving the thin film 636 patterned by the combination  
5 of fixed mask and discretionary E-Beam or Ion-Beam method.  
6 This method is applicable to both metal and dielectric thin  
7 films.

8 Figures 39(a) through 39(d) show the patterning of a  
9 discretionary area of thin film 658 on substrate 652 with  
10 application of positive E-Beam or Ion-Beam resist. The  
11 resist area exposed by the E-Beam or Ion-Beam is removed by  
12 development of the resist, and therefore, unexposed resist  
13 is used to protect the previously patterned metal traces  
14 while patterning the metal film of the discretionary area.  
15

16 Positive E-Beam or Ion-Beam resist 654 is applied in  
17 Figure 39(a) and exposed with a discretionary pattern 656  
18 over unpatterned areas of thin film 658-2 as determined by  
19 the tester in a previous processing step. The resist is  
20 developed in Figure 39(b) leaving a pattern 660 to be etched  
21 into the unpatterned thin film 658-2 while the rest of the  
22 patterned thin film layer 658-1 is protected from the etch  
23 processing step by overlying resist 654. The pattern is  
24 etched in Figure 39(c). Resist areas 654, 660 are stripped  
25 in Figure 39(d) leaving discretionary patterns 664 with the  
26 portion of the thin film pattern by the fixed mask  
27 unaffected. This method is applicable to both metal and  
28 dielectric thin films.

29 Figures 39(a) through 39(d) thus show in cross-section  
30 the use of positive E-Beam or Ion-Beam resist to pattern a  
31 discretionary area while simultaneously protecting a pre-  
32 existing metal pattern. This method does not require a  
33 prior application of a resist to protect the existing metal  
34 pattern as shown in Figures 38(a) through 38(d).

35 The fine-grain testing capability of the tester allows  
36 the determination of a small area (typically less than  
37 100  $\mu\text{m}$  on a side) for discretionary patterning. The use of  
38 an optical stepper exposure under computer control  
determines the size and placement of rectangular exposure

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1 areas derived from the tester device database in combination  
2 with the various optical resists and prevents the patterning  
3 of the dielectric or metal film deposited over defective  
4 ICLUs after the initial pattern exposure of the resist by a  
5 fixed mask. Only these resulting unpatterned film areas  
6 over the defective ICLUs must subsequently be patterned by  
7 E-Beam or Ion-Beam processing rather than the complete  
8 pattern layer. This reduces the use of an E-Beam or  
9 Ion-Beam exposure to a limited area of the total substrate,  
10 typically less than 1%, and therefore, significantly lowers  
11 the cost that normally would be anticipated with using  
12 E-Beam or Ion-Beam equipment.

13 When etching a dielectric layer in a discretionary area  
14 predetermined by the tester, the resist used may vary from  
15 that described above for patterning a conductive or metal  
16 film. It may be more efficient to use a positive or  
17 negative resist when forming vias in a dielectric layer  
18 where metal film may require the opposite resist type.

19 Computer Aided Design (CAD) rip-up router software uses  
20 the defect database of the integrated circuit determined by  
21 the tester in accordance with the invention and the original  
22 placement and routing database of the circuit to generate  
23 the new patterns for the fine-grain discretionary areas to  
24 be patterned. These newly determined patterns become input  
25 control information to E-beam, Ion-Beam or optical exposure  
26 equipment, or as will be described below, Ion-Beam film  
27 deposition/etch patterning equipment.

28

29        Ion Beam For IC Wiring

30        Ion-beam film deposition or etch processing offers a  
31 potential cost reduction over the above-described E-beam or  
32 Ion-Beam exposure technique for completing the fine-grain  
33 discretionary wiring of an IC. Whereas E-beam and Ion-Beam  
34 are used to create fine-grain discretionary patterning in  
35 conjunction with the application of an existing master mask  
36 (reticle), either as a separate physical mask (the master  
37 reticle modified with required local fine-grain  
38 discretionary patterning changes) or as a direct-write on

1 wafer resist exposure mask step as provided above, the Ion-  
2 beam equipment can be used locally (in a fine-grain manner)  
3 to directly etch a dielectric thin film layer, or deposit  
4 dielectric or metal thin films, requiring no additional  
5 resist, deposition and etching steps. Ion-beam, like  
6 E-beam, is slower in processing time relative to optical  
7 exposure techniques, and offers equivalent sub-micron  
8 precision and pattern geometries. The method in accordance  
9 with the invention only requires routing changes that are  
10 local to an area typically less than 100 $\mu$ m in diameter. The  
11 Ion-beam means makes the necessary discretionary wiring  
12 route changes on a layer-by-layer basis after the  
13 application of the fixed mask associated with a specific  
14 layer. Ion-beam processing equipment is presently much  
15 cheaper than E-beam equipment, and available from several  
16 sources; the Ion-beam equipment of most recent note is the  
17 Seiko SMI-8100 which is suitable for use in accordance with  
18 the invention.

19       The application of the Ion-Beam means for the patterning  
20 of metal and dielectric (or passivation) thin films in  
21 conjunction with an optical stepper means as described above  
22 does not require the application of a negative resist or  
23 combined use of two resist layers. Figures 40(a) through  
24 40(e) show in cross-section the use of positive optical  
25 resist to pattern a thin metal film 680 formed on substrate  
26 682 with a fixed mask, and a second optical exposure (as  
27 described previously) over a discretionary area to blank out  
28 that portion of the fixed mask pattern and allow the  
29 underlying metal film to be etched away. In a subsequent  
30 processing step Ion-Beam equipment is used to deposit a  
31 metal trace pattern in the discretionary area which was  
32 etched free of the original thin metal film during the fixed  
33 mask patterning step. The Ion-Beam equipment directly  
34 closes or etches open vias in the dielectric thin film layer  
35 specific to the size and placement data derived from the  
36 tester means database and the CAD circuit database.

38       Positive optical resist 684 is applied in Figure 40(a)  
over thin film 680 and portions 686 exposed by a fixed mask

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1 (not shown). Areas 688 of the thin film (see Figure 40(b))  
2 that require discretionary patterning, as determined by the  
3 tester, are given a second exposure (by shutter controlled  
4 maskless optical stepper equipment) to erase the pattern  
5 created by the fixed exposure. Resist 684 is developed in  
6 Figure 40(c) and the resist pattern etched into the thin  
7 film 690, and the discretionary areas 692 are etched free of  
8 the thin film layer. The resist is stripped in Figure 40(d)  
9 leaving the unaffected portions of the thin film 694  
10 patterned by the fixed mask. Discretionary thin film  
11 depositions 696 are then made by the Ion-Beam in the  
12 discretionary areas 692, completing the patterning of the  
13 film. This method can be applied to dielectric layers in  
14 the same manner, except a negative resist is used in this  
15 case and the Ion-Beam means etches openings (vias) in the  
16 dielectric layer rather than depositing metal.

17 Discretionary metal patterns are directly deposited on  
18 the substrate by the Ion-Beam equipment. This requires that  
19 the rectangular areas in which discretionary patterning is  
20 to be performed be etched free of the metal film deposited  
21 for the fixed mask optical exposure patterning step. This  
22 is done by a separate optical stepper exposure step wherein  
23 the shutter of the stepper is positioned and set to open to  
24 the size of the rectangular areas identified for  
25 discretionary metal patterning and stepper control  
26 information is derived from the tester means defective ICLU  
27 database. The rectangular areas requiring discretionary  
28 patterning are etched clear of any deposited metal in the  
29 same step that the fixed mask patterning of the remaining  
30 areas of the metal film is processed. The Ion-Beam  
31 equipment subsequently deposits the desired discretionary  
32 metal traces from control data derived from the CAD rip-up  
33 router circuit database, computed specifically from the  
34 results in the tester means database which determined the  
35 areas that required discretionary patterning, into the  
36 rectangular areas that were etched clear of deposited metal  
37 film as shown in Figures 40(a) through 40(e), or etches  
38 required via openings in a dielectric layer.

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1        Discretionary Interconnect with only First Via Layer  
2        Modification

3        Discretionary patterning modification limited only to  
4 the first via layer which separates ICLUs or circuit device  
5 elements from metal layer interconnections is sufficient to  
6 avoid connecting defective ICLUs or circuit device elements  
7 when there is complete redundancy of all ICLUs or circuit  
8 device elements. Metal traces are patterned as if to  
9 simultaneously interconnect primary and redundant circuit  
10 devices. The vias in the first dielectric via layer are  
11 only patterned (by fixed mask) to connect the primary device  
12 and not its redundant equivalent. If the tester determines  
13 that a primary device is defective, the vias corresponding  
14 to that primary device are closed or not opened, and vias  
15 corresponding to its redundant equivalent are opened. This  
16 isolates the defective device and connects its replacement  
17 without the need to change metallization patterning. The  
18 modification of the vias can be effected through local  
19 application of Ion-Beam equipment as described below using  
20 control data derived from the tester database and shown in  
21 cross-section by Figures 41(a) through 41(c).

22        Defective ICLU 700 formed on substrate 702 in Figure  
23 41(a) is determined by the tester, and replaced by redundant  
24 ICLU 704. Vias 706 formed in a dielectric layer 708  
25 allowing contact to the electrodes of a defective ICLU 700  
26 are closed in Figure 41(b) by dielectric deposition 710 in  
27 the vias 706 by Ion-Beam equipment. Vias 712 to the  
28 electrodes of designated replacement (redundant) ICLU 704  
29 are opened by Ion-Beam equipment etching of the dielectric  
30 layer 708. Subsequent thin film metal deposition 714, 716  
31 in Figure 41(c) and patterning by fixed mask is made  
32 respectively to the closed vias 706 of defective ICLU 700  
33 and the opened vias 712 of the redundant ICLU 704.

34        Figures 41(a) through 41(c) thus show in cross-section  
35 discretionary modification to a dielectric layer to prevent  
36 metal trace connection of a defective transistor, and to  
37 cause the connection of a spare (redundant) transistor to  
38 replace the defective transistor. This method does not

1 require discretionary modification of the metal layer  
2 patterns or resist based patterning steps, but does require  
3 100% redundancy of all transistors with a metallization  
4 interconnect pattern for the primary transistor and its  
5 replacement spare, and with vias in the dielectric layer  
6 that provide connection only for the primary transistor.  
7 The tester means determines if the primary transistor is  
8 defective, and if it is, provides control data for the  
9 closing of the vias of the primary transistor and etching of  
10 the vias in the dielectric layer of the spare transistor by  
11 an Ion-Beam. (E-Beam and optical equipment can also be used  
12 to make discretionary via patterns in dielectric layers as  
13 shown above.)

14 Complete redundancy of circuit ICLU or device elements  
15 has practical application in logic and analog circuits where  
16 the order of the devices of the IC are not regular, or in  
17 flat panel display (e.g., Active Matric LCD) or imaging  
18 arrays where the density of ICLUs or circuit devices is  
19 low. This method of discretionary interconnect  
20 significantly simplifies the number of manufacturing steps  
21 to achieve discretionary interconnect. It does, however,  
22 come with the added cost of 100% or greater redundancy.  
23 There is a savings in this because logic circuits with  
24 redundancy do not require a correspondingly proportional  
25 increase in the area of an IC versus a circuit with no  
26 redundancy; this is due largely to the fact that the active  
27 device elements of logic circuits occupy typically less than  
28 25% of the substrate area of an IC, the rest of the area is  
29 used by interconnect metallization.  
30

31 The Testing and Localized Repair of Metallization Layers  
32 The following describes the use of the tester in the  
33 testing and repair of via and metal layers of an IC. The  
34 tester method for testing that a via is open to a lower  
35 conductive layer is to place a probe point tip into the via  
36 and to make contact with the bottom of the via; or to  
37 deposit metallization into the via by means of standard  
38 metal deposition and etching techniques, and then using the

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1 tester to test electrical continuity among some number of  
2 mutually connected vias. Metal traces are tested with a  
3 tester by positioning probe points for contact among some  
4 number of metal traces that allow determination of the  
5 independent continuity of the various traces being  
6 contacted. The CAD database for the circuit is used to  
7 determine in an automated fashion the placement of the probe  
8 points during the fabrication of the tester surface, and the  
9 interconnection of the probe points with tester means logic  
10 is as described above.

11 The tester means fine-grain determination of a defective  
12 via or metal trace is followed by two preferred methods for  
13 remedy of the defects: 1) complete reprocessing of the  
14 whole substrate layer; or 2) local reprocessing of only the  
15 defective portion of the layer. The complete reprocessing  
16 of the substrate is performed with conventional IC  
17 processing such as etch removal of a patterned layer and  
18 redepositing and patterning it; the novel processing step  
19 being the use of the tester means to perform 100% testing of  
20 the substrate layer to determine whether substrate layer  
21 reprocessing is required. The reprocessing of a complete  
22 substrate layer may correct a specific metallization defect,  
23 but may also have a reasonable probability of introducing a  
24 new metallization defect. The local correction of  
25 metallization or via defects for a particular metal  
26 interconnect layer greatly reduces the probability that a  
27 new defect will be introduced.

28 Figures 42(a) through 42(b) show in cross-section the  
29 use of Ion-Beam equipment to repair either a defective metal  
30 trace or via in a dielectric layer on a substrate 722 as  
31 determined by the tester. The defects are determined by the  
32 tester means, and the database formed by the tester means  
33 provides the positioning data for the Ion-Beam means to  
34 process the defects.

35 Defective metal traces 724 in Figure 41(a) (caused by a  
36 break 726 in the trace 724) and located by the tester means  
37 are repaired by Ion-Beam deposition of metal along the metal  
38 trace 724. The metal deposition in Figure 32(b) of the

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1 Ion-Beam fills the break 726 in the defective trace 724 by  
2 depositing a new metal trace 728 over the length of the  
3 existing defective metal trace 724.

4 Defective dielectric vias 732 in Figure 42(c) in  
5 dielectric thin films 734 found by the tester are incomplete  
6 openings in the dielectric layer 734 to an electrode 736 in  
7 a lower layer. The incomplete via 732 is opened in Figure  
8 42(d) by Ion-Beam equipment by etch removal of dielectric  
9 material 734 and so to complete the via opening 738.

10 Repair of defective via and metal trace patterning is  
11 not limited to the Ion-Beam deposition/etch method  
12 described, but application of resist with localized exposure  
13 E-Beam, Ion-Beam or optical exposure and etching of  
14 dielectric or metal thin films can also be used.

15

16 Fuses and Anti-Fuse Discretionary Interconnection

17 The tester means in accordance with the invention is  
18 used in one embodiment to access and blow fuses (i.e., open  
19 a metal trace or disconnect a metal trace) or anti-fuses  
20 (i.e., close or connect two metal traces) as a discretionary  
21 method of forming interconnections in a IC. This process is  
22 employed after a circuit is fabricated and prior to  
23 packaging in order to configure the final internal metal  
24 interconnections as in the case of PLAs (programmable logic  
25 arrays), or in circuit repair after functional IC testing.  
26 The tester used as a circuit programmer in the final steps  
27 of IC fabrication simplifies the design of the circuit since  
28 the tester probe points contact immediately adjacent to the  
29 fuse or antifuse device, and therefore, no additional  
30 interconnect traces or control logic internal to the circuit  
31 are required for access to the fuse/antifuse device. This  
32 gives the capability to make incremental corrections without  
33 obsoleting manufacturing tooling or inventory. The tester  
34 means contacts small metal contacts (less than 1 mil square)  
35 positioned as appropriate (i.e., arbitrarily) anywhere on  
36 the surface of the IC which would directly access the  
37 electrodes of a fuse or anti-fuse or metal traces  
38 (electrodes) of a fuse or anti-fuse device. The tester then

1 applies the appropriate voltage at the metal contacts to  
2 blow the fuse or anti-fuse device.

3 The use of fuses and anti-fuses may also be used to  
4 disconnect and/or connect ICLUs from a circuit during  
5 manufacturing. The tester means, once it has determined  
6 that an ICLU is defective, is directed to break or make  
7 associated fuse and anti-fuse links in the same step or in a  
8 subsequent manufacturing step.

9

**10 BURN-IN TESTING**

11 The tester in accordance with the invention in its  
12 implementation with integrated logic in the tester surface  
13 is significantly cheaper to manufacture than present IC  
14 testing systems. This lower cost is consistent with the  
15 familiar historical cost savings that have resulted from use  
16 of higher levels of circuit integration. The lower cost of  
17 the present invention in combination with its ability to  
18 provide extremely high probe point counts with geometries of  
19 1 mil diameter or less provides a cost effective method in  
20 accordance with the invention to be used for burn-in of the  
21 ICLUs or circuit devices prior to completion of IC  
22 fabrication (i.e., prior to circuit device metallization  
23 interconnection).

24 Burn-in of ICLUs or circuit devices is accomplished by  
25 applying the tester to the DUT over extended periods of  
26 time, such as several seconds to several hours or several  
27 days or longer. The mechanical contact process of the  
28 tester is unchanged; however, the area of the DUT that is  
29 processed per contact would be maximized and the mechanical  
30 operation of the tester head equipment simplified so as to  
31 contact only one area of the DUT substrate, and therefore,  
32 lower equipment costs. The burn-in of ICLUs includes the  
33 operation of the ICLUs under stressing voltage and/or  
34 current loading. During the extended time that a tester  
35 means is in contact with the DUT, the ICLUs of the DUT are  
36 periodically tested repeatedly or biased at a voltaged level  
37 in a static condition.

38

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1        The ability of the burn-in method in accordance with the  
2 invention to tolerate higher average operating temperatures  
3 (since the materials used in the fabrication of the tester  
4 surface are stable to temperatures in excess of 200° C)  
5 allows the ICLUs to be subjected to what is called  
6 accelerated aging by operation of the ICLUs at elevated  
7 temperatures (i.e., 25° to 150° C or more over normal  
8 ambient temperature); this is a standard military functional  
9 qualification method for completed ICs. Burn-in and burn-in  
10 with accelerated aging have been found to extend the MTTF  
11 (Mean Time To Failure) of a system by causing the marginal  
12 IC components of the system which would most likely fail in  
13 the first twenty-four months of operation to fail before the  
14 system begins its useful life. ICLUs can be tested in this  
15 fashion in accordance with the invention and provide  
16 increased MTTF at the IC component level without significant  
17 change to the procedures of ICLU testing.

18       This method includes the use of the tester means to  
19 perform a function in addition to testing. The tester means  
20 is brought into prolonged contact with a large number of  
21 ICLUs under stressing electrical and thermal conditions in  
22 an effort to cause those ICLUs or device elements of  
23 marginal manufacture to fail. This is a novel reliability  
24 assurance manufacturing step.

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1 CLAIMS

2

3 I claim:

4

5 1. A method of testing an integrated circuit  
6 comprising the steps of:7 electrically contacting each one of a plurality of  
8 devices in the integrated circuit;9 applying an electrical current to each one of the  
10 devices for a period of at least one second; and11 determining after the period if each of the devices  
12 is functional.

13

14 2. The method of Claim 1, further comprising the step  
15 of elevating an ambient temperature of the integrated  
16 circuit by at least 25°C.

17

18 3. The method of Claim 1, further comprising, after  
19 the step of determining, the step of interconnecting the  
20 devices.

21

22 4. A method for providing discretionary  
23 interconnections in an integrated circuit comprising the  
24 steps of:25 providing a plurality of discretionary metal traces  
26 each being in a conductive or in a nonconductive state  
27 in the integrated circuit, each metal trace being  
28 contacted at each of its two ends by a metal contact  
29 less than one mil by one mil in size; and30 contacting the two contacts at the ends of one  
31 trace and applying a voltage to the two contacts so a  
32 current flows through the metal trace, thereby causing  
33 the trace to change its state into the other state.

34

35 5. The method of Claim 4, further comprising the step  
36 of testing the metal traces during the fabrication of the  
37 interconnections of an integrated circuit.

38

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1        6. A method of testing an integrated circuit  
2 comprising the steps of:  
3                providing a tester having a plurality of probe  
4                points on a first side of the tester;  
5                electrically contacting devices in the integrated  
6                circuit with the probe points;  
7                vibrating the tester so as to achieve improved  
8                electrical contact; and  
9                electrically testing the devices by providing  
10               signals to the devices through the probe points.

11  
12        7. The method of Claim 6, further comprising the steps  
13 of:  
14               providing a fluid on a second side of the tester;  
15               and  
16               vibrating the fluid so as to vibrate the tester.

17  
18        8. The method of Claim 6, further comprising the steps  
19 of:  
20               providing a piezoelectric layer on a second side of  
21               the tester; and providing a varying electrical signal to  
22               the piezoelectric layer so as to vibrate the tester.

23  
24        9. A tester surface comprising:  
25               a substrate having formed on it a plurality of  
26               probe points;  
27               a first plurality of parallel traces connecting to  
28               the probe points formed on the substrate;  
29               a second plurality of parallel traces formed on the  
30               substrate perpendicular to the first plurality of traces  
31               connecting to the probe points; and  
32               means for providing test signals to and receiving  
33               test signals from the first and second plurality of  
34               traces.

35  
36        10. The device of Claim 9, wherein the means for  
37               providing includes integrated circuitry mounted on the  
38               tester surface.

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1

2 11. The device of Claim 9, further comprising means for  
3 selectively controlling a voltage of a test signal applied  
4 to any of the plurality of probe points.

5

6 12. A tester surface comprising:  
7 a substrate formed of a first layer of flexible  
8 material; and

9 a plurality of probe points extending from the  
10 substrate, each probe point including an elongated core  
11 of conductive metal surrounded by a second layer of  
12 flexible material which extends over the first layer of  
13 flexible material; wherein each probe point is capable  
14 of bending at least 10% of its length.

15

16 13. The device of Claim 12, wherein each probe point  
17 includes a metal tip formed on an end of the core farthest  
18 from the substrate, the tip being of a greater diameter than  
19 is the core and being in electrical contact with the core.

20

21 14. The device of Claim 12, wherein both the first  
22 layer and second layer comprise low stress silicon dioxide.

23

24 15. The device of Claim 12, wherein the first layer  
25 comprises a polymer film less than 10  $\mu\text{m}$  thickness.

26

27 16. The device of Claim 12, wherein the tester surface  
28 includes at least 1000 probe points.

29

30 17. The device of Claim 12, wherein each probe point  
31 has a maximum outside diameter of less than one mil.

32

33 18. The device of Claim 12, wherein the core defines an  
34 interior cavity filled with a flexible material.

35

36 19. The device of Claim 12, wherein the core defines an  
37 interior cavity filled with a polymer.

38

1        20. The device of Claim 12, further comprising a rigid  
2 substrate layer on which said first layer of flexible  
3 material is formed.

4

5        21. A tester surface comprising:  
6                a substrate formed of a flexible material;  
7                a plurality of probe points extending from the  
8                substrate, each probe point including an outer layer of  
9                flexible material defining a cavity and having an inner  
10               layer of conductive metal formed on the outer layer,  
11               wherein the outer layer is joined to the substrate,  
12               wherein the probe point is compressible by at least 10%  
13               of its length.

14

15        22. The device of Claim 21, wherein the cavity of each  
16 probe point is filled with a fluid.

17

18        23. The device of Claim 21, wherein the cavity of each  
19 probe point is filled with an elastomeric polymer.

20

21        24. The device of Claim 21, wherein each probe point  
22 includes a metal tip formed on an end of the probe point  
23 farthest from the substrate, the tip being in electrical  
24 contact with the inner layer.

25

26        25. The device of Claim 21, wherein both the substrate  
27 and the outer layer comprise low stress silicon dioxide.

28

29        26. The device of Claim 21, wherein the substrate  
30 comprises a polymer film less than 10  $\mu$ m in thickness.

31

32        27. The device of Claim 21, wherein the tester surface  
33 includes at least 1000 probe points.

34

35        28. The device of Claim 21, wherein each probe point  
36 has a maximum outside diameter of less than one mil.

37

38        29. The device of Claim 21, further comprising a rigid

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1 substrate layer on which said first layer of flexible  
2 material is formed.

3

4       30. A tester head assembly comprising:  
5            an enclosure defining an interior cavity;  
6            a tester surface having a plurality of probe points  
7            extending from one side of the surface, a second side of  
8            the tester surface being in contact with the cavity;  
9            a plurality of electrical contacts formed on the  
10          enclosure and in electrical contact with the probe  
11          points; and  
12            means for providing liquid to the cavity.  
13

14       31. The device of Claim 30, further comprising at least  
15       one integrated circuit formed on the enclosure for providing  
16       electrical signals to the probe points.  
17

18       32. The device of Claim 30, further comprising  
19       electrical contacts formed on the enclosure of a conductive  
20       elastomeric polymer.  
21

22       33. A method of making a tester surface comprising the  
23       steps of:  
24            providing a substrate having a principal surface;  
25            forming a plurality of cavities in the substrate  
26            each extending from the principal surface to a depth in  
27            the substrate;  
28            lining the cavities and covering the principal  
29            surface with a first layer of a flexible material;  
30            providing a first layer of metal on the first layer  
31            of flexible material lining the cavities and over at  
32            least a portion of the principal surface overlying the  
33            first layer of flexible material;  
34            forming a second layer of a flexible material over  
35            the principal surface and overlying the first layer of  
36            metal;  
37            removing a portion of the substrate adjacent to the  
38            depth of each cavity so as to expose a portion of the

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1       first layer of flexible material at the depth of the  
2       cavity;  
3           removing the exposed portion of the first layer of  
4       flexible material, so as to expose a portion of the  
5       first layer of metal;  
6           forming a metal tip on the exposed portion of the  
7       metal layer; and  
8           removing the remaining portion of the substrate.  
9

10       34. The method of Claim 33, further comprising after  
11      the step of providing the first layer of metal, the steps  
12     of:

13           filling the cavity with additional flexible  
14       material, the additional flexible material extending  
15       over the principal surface; and  
16           forming a second layer of metal over a portion of  
17       the additional flexible material extending over the  
18       principal surface.  
19

20       35. The method of Claim 33, further comprising, after  
21      the step of providing the first layer of metal, the steps  
22     of:

23           forming a third layer of flexible material on the  
24       cavity and on the principal surface overlying the first  
25       layer of metal;  
26           forming a body of metal in the depth of the cavity;  
27           overlying the third layer of flexible material; and  
28           forming a second layer of metal over a portion of  
29       the third layer of flexible material overlying the  
30       principal surface.  
31

32       36. The method of Claim 33 wherein the step of forming  
33      the plurality of cavities comprises:

34           providing a computer data base for determining a  
35       location where each cavity is to be formed in the  
36       substrate;  
37           forming a mask from the locations in the database;  
38           using the mask to delineate the location on the

- 59 -

1       substrate for each cavity; and  
2               forming a cavity in each delineated location.

3

4       37. A method of repairing incomplete vias in an  
5 integrated circuit structure comprising the steps of:  
6               locating an incomplete via formed in a dielectric  
7               layer of the structure; and  
8               etching away a portion of the dielectric layer in  
9               the via by an ion-beam.

10

11       38. The method of Claim 37 further comprising the step  
12 of etching away of a portion of the dielectric layer by  
13 patterning a resist with an ion-beam or E-beam.

14

15       39. A method of repairing defective traces in an  
16 integrated circuit structure comprising the steps of:  
17               locating a trace having a defective portion; and  
18               depositing metal by an ion-beam over the defective  
19               portion.

20

21       40. The method of Claim 39, wherein the steps of  
22 depositing of metal over the defective portion comprises the  
23 step of depositing through a patterned resist layer.

24

25       41. A method of making an integrated circuit  
26 interconnection comprising the steps of:  
27               forming a conductive film on a substrate;  
28               applying a layer of negative resist over the  
29               conductive film;  
30               patterning the negative resist layer with a fixed  
31               mask;  
32               exposing predetermined portions of the resist over  
33               particular portions of the conductive film using an  
34               optical stepper without a mask;  
35               developing the resist layer; and  
36               etching away the portions of the conductive film  
37               underlying unexposed portions of the resist layer.

38

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1       42. A method of making an integrated circuit  
2 interconnection comprising the steps of:  
3           forming a dielectric film on a substrate;  
4           applying a layer of negative resist over the  
5 dielectric film;  
6           patterning the negative resist layer with a fixed  
7 mask;  
8           exposing predetermined portions of the resist over  
9 particular portions of the dielectric film using an  
10 optical stepper without a mask;  
11          developing the resist layer; and  
12          etching away the portions of the dielectric film  
13 underlying unexposed portions of the resist layer.  
14

15       43. A method of making an integrated circuit  
16 interconnection comprising the steps of:  
17           forming a conductive film on a substrate;  
18           applying a layer of negative resist over the  
19 conductive film;  
20           exposing predetermined portions of the resist layer  
21 by use of an optical stepper without a mask;  
22          developing the resist layer;  
23          applying a layer of positive resist over the  
24 negative resist layer;  
25          patterning the positive resist layer with a fixed  
26 mask; and  
27          removing any remaining portions of the negative  
28 resist layer and positive resist layer.  
29

30       44. A method of making an integrated circuit  
31 interconnection comprising the steps of:  
32           forming a dielectric film on a substrate;  
33           applying a layer of negative resist over the  
34 dielectric film;  
35           exposing predetermined portions of the resist layer  
36 by use of an optical stepper without a mask;  
37          developing the resist layer;

1                   applying a layer of positive resist over the  
2                   negative resist layer;  
3                   patterning the positive resist layer with a fixed  
4                   mask; and  
5                   removing any remaining portions of the negative  
6                   resist layer and positive resist layer.

7

8       45. A method of making an integrated circuit  
9   interconnection comprising the steps of:  
10               forming a patterned film on a substrate;  
11               applying a layer of positive optical resist over  
12               the patterned film;  
13               exposing portions of the positive optical resist  
14               layer by use of an optical stepper without a mask;  
15               developing the positive optical resist layer;  
16               applying a negative non-optical resist over the  
17               developed positive optical resist layer;  
18               exposing predetermined portions of the negative  
19               resist layer by use of a beam;  
20               developing the exposed portions of the negative  
21               resist layer;  
22               removing any portions of the film underlying  
23               non-exposed portions of the negative resist layer; and  
24               removing any remaining portions of the positive  
25               optical resist layer and negative resist layer.

26

27       46. A method of making an integrated circuit  
28   interconnection comprising the steps of:  
29               forming a patterned film on a substrate;  
30               applying a layer of positive optical resist over  
31               the patterned film;  
32               exposing portions of the positive optical resist  
33               layer by use of an optical stepper without a mask;  
34               developing the positive optical resist layer;  
35               applying a positive non-optical resist over the  
36               developed positive optical resist layer;  
37               exposing predetermined portions of the positive  
38               resist layer by use of a beam;

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1           developing the non-exposed portions of the positive  
2           resist layer;  
3           removing any portions of the film underlying  
4           exposed portions of the positive resist layer; and  
5           removing any remaining portions of the positive  
6           resist layers.

7

8        47. A method of making an integrated circuit  
9 interconnection comprising the steps of:

10        forming a patterned conductive layer on a  
11        substrate;  
12        applying a layer of positive non-optical resist  
13        over the conductive layer;  
14        exposing predetermined portions of the positive  
15        resist;  
16        developing the positive resist layer;  
17        etching a pattern into the portions of the  
18        conductive film underlying the exposed predetermined  
19        portions of the positive resist layer; and  
20        removing any remaining portions of the positive  
21        resist layer.

22

23        48. A method of making an integrated circuit  
24 interconnection comprising the steps of:

25        forming a patterned dielectric layer on a  
26        substrate;  
27        applying a layer of positive non-optical resist  
28        over the dielectric layer;  
29        exposing predetermined portions of the positive  
30        resist;  
31        developing the positive resist layer;  
32        etching a pattern into the portions of the  
33        dielectric film underlying the exposed predetermined  
34        portions of the positive resist layer; and  
35        removing any remaining portions of the positive  
36        resist layer.

37

38

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1       49. A method of making an integrated circuit  
2 interconnection comprising the steps of:  
3           forming a conductive film on a substrate;  
4           applying a layer of positive optical resist over  
5       the film;  
6           exposing the resist layer by use of a fixed mask;  
7           exposing predetermined portions of the resist layer  
8       by an optical stepper without use of a mask;  
9           developing the resist layer;  
10          etching away portions of the film underlying the  
11       exposed portions of the resist layer;  
12          removing any remaining portions of the resist  
13       layer; and  
14           patterning the remaining portions of the film by  
15       use of an ion-beam.

16  
17       50. A method of making an integrated circuit  
18 interconnection comprising the steps of:  
19           forming a dielectric film on a substrate;  
20           applying a layer of negative optical resist over  
21       the film;  
22           exposing the resist layer by use of a fixed mask;  
23           exposing predetermined portions of the resist layer  
24       by an optical stepper without use of a mask;  
25           developing the resist layer;  
26          etching away portions of the film underlying the  
27       non-exposed portions of the resist layer;  
28          removing any remaining portions of the resist  
29       layer; and  
30           patterning the remaining portions of the film by  
31       use of an ion-beam.

32  
33       51. A tester surface comprising:  
34           a substrate formed of a flexible material;  
35           a plurality of probe points extending from a first  
36       side of the substrate; and  
37           a layer of conductive elastomeric polymer formed on  
38       a second side of the substrate.

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1

2        52. The device of Claim 51, wherein conductive  
3        elastomeric polymer is formed on a second side of the  
4        substrate by electroplating.

5

6        53. The device of Claim 51, further comprising a layer  
7        of low stress polysilicon formed on those portions of the  
8        second side of the substrate extending between adjacent  
9        probe points.

10

11       54. The device of Claim 51, further comprising a layer  
12       of metal formed on a side most distant from the substrate of  
13       the layer of conductive elastomeric polymer.

14

15       55. A tester surface comprising a plurality of probe  
16       points, where each probe point includes one or more circuit  
17       devices for controlling signals to the probe point or from  
18       the probe point.

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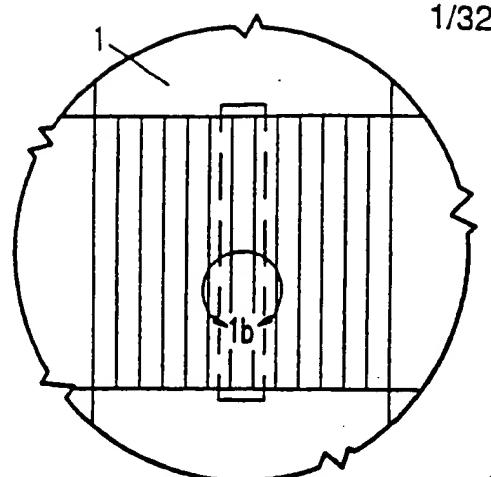


FIG. 1a

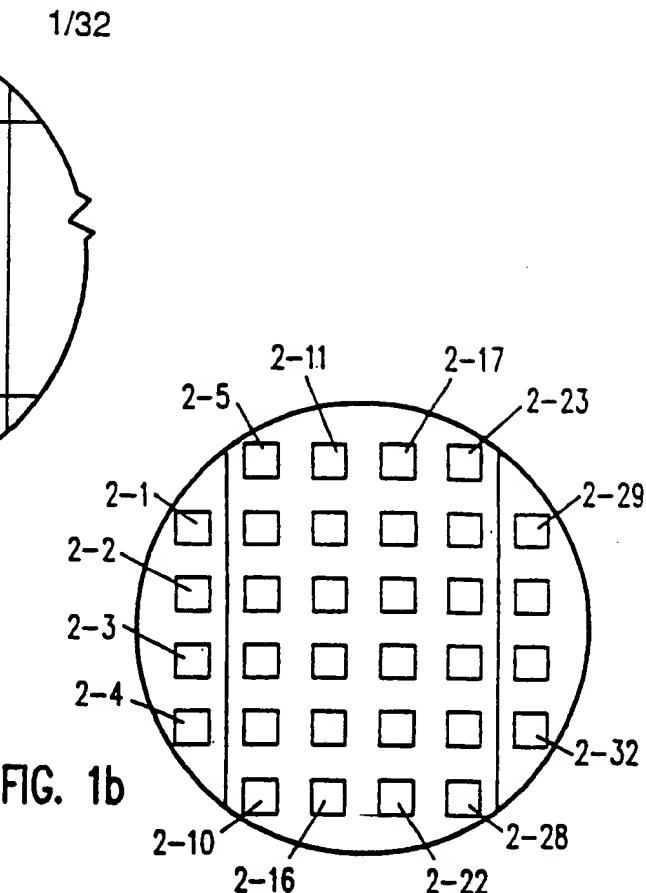


FIG. 1b

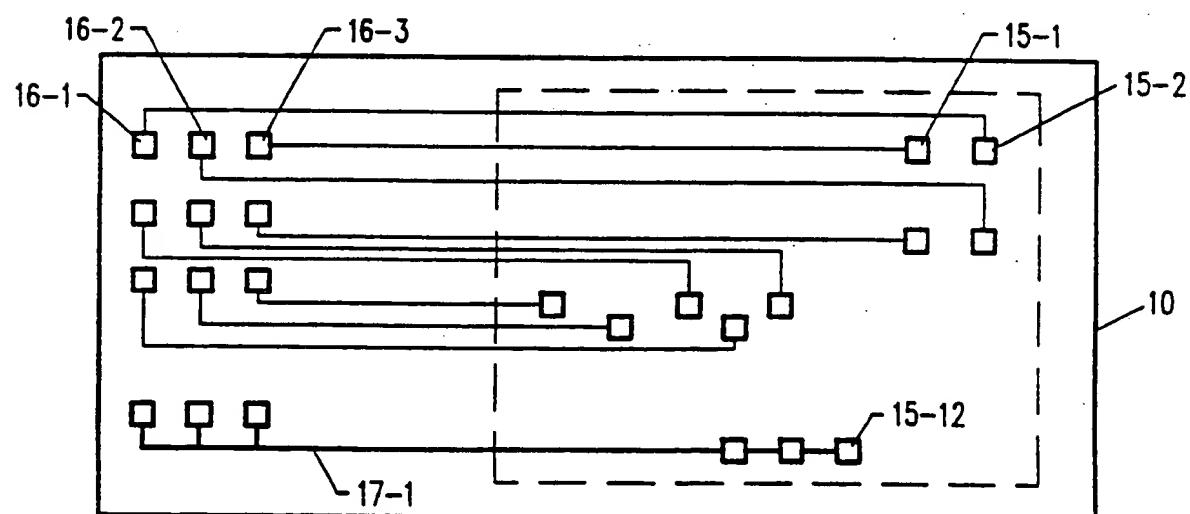


FIG. 2

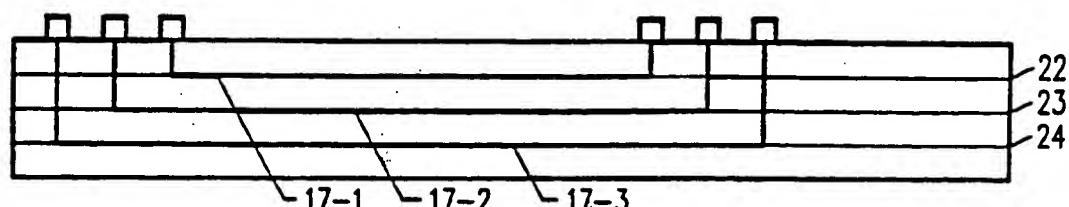


FIG. 3

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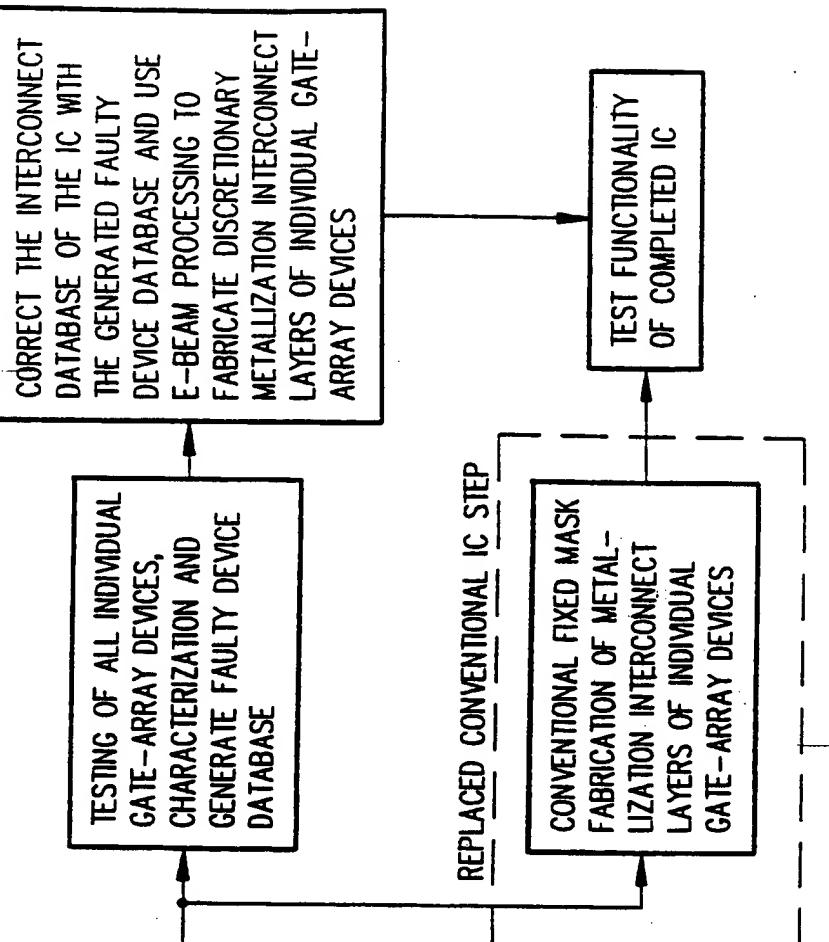


FIG. 4b

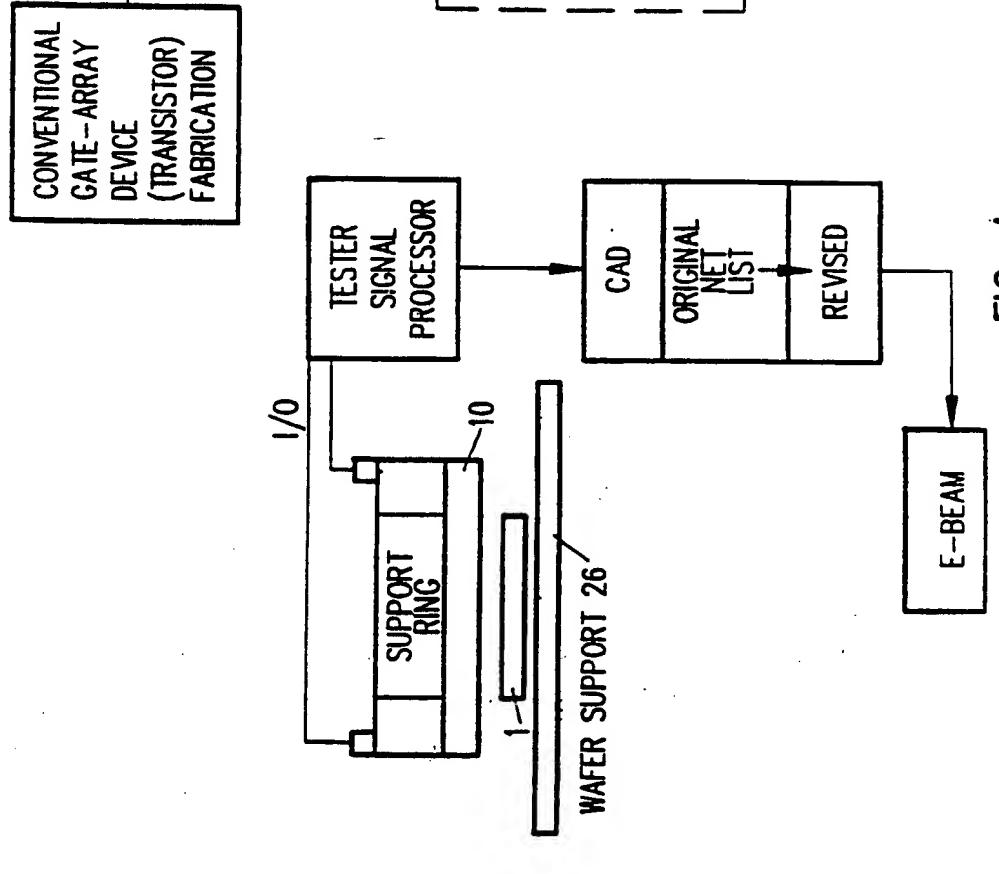


FIG. 4a

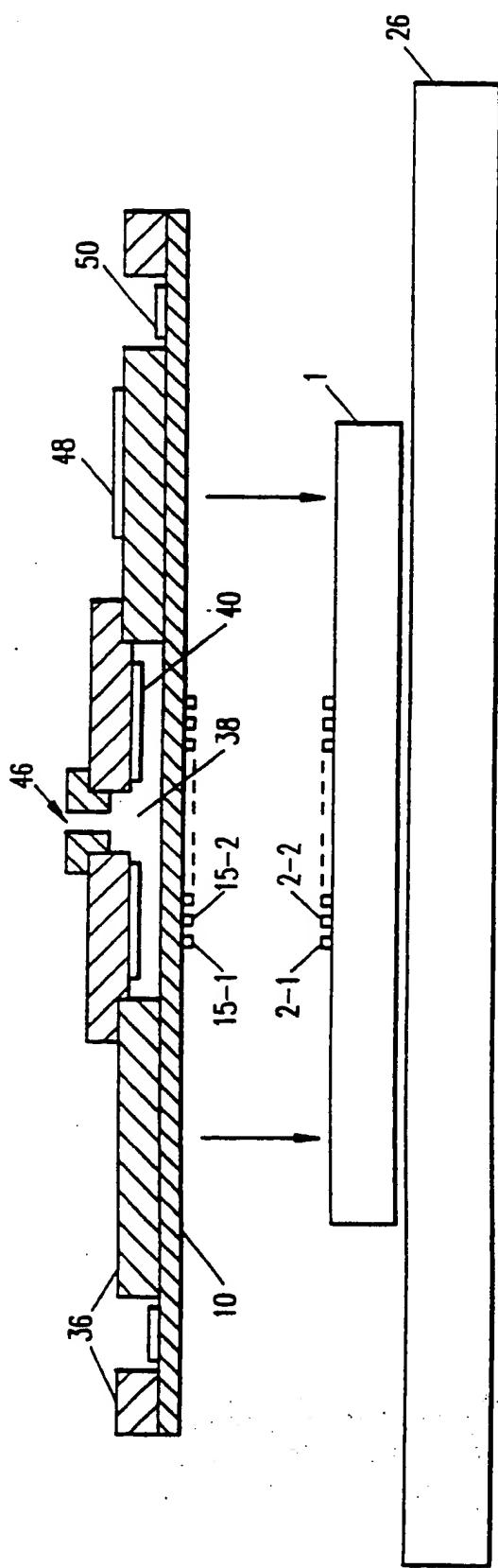


FIG. 5

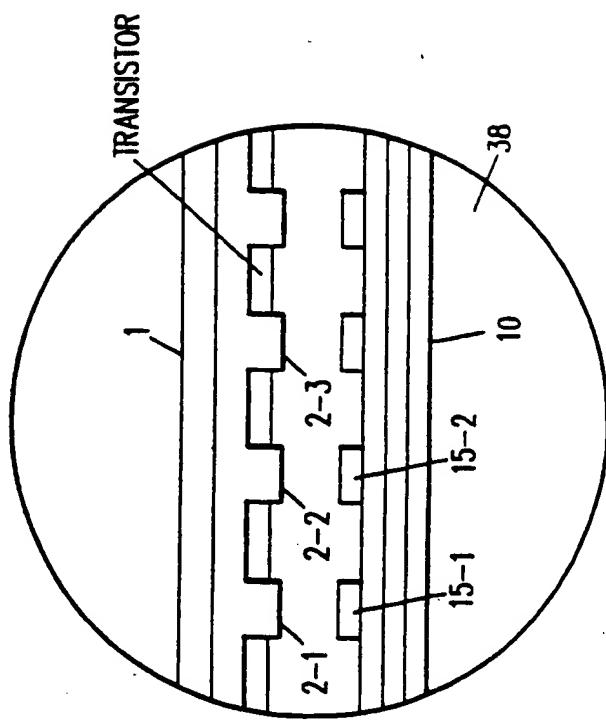


FIG. 6

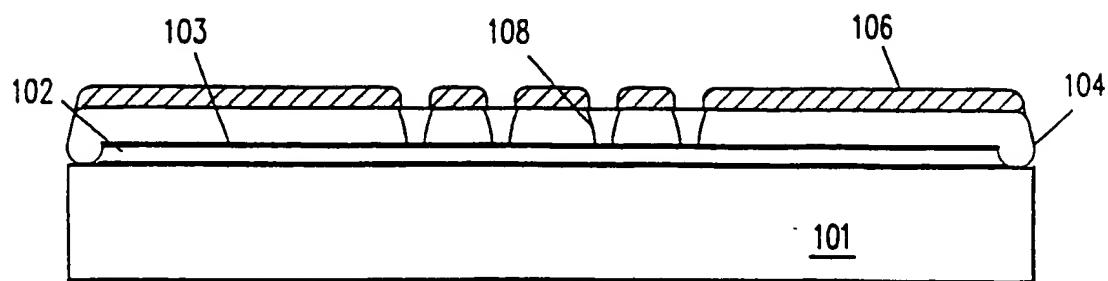


FIG. 7

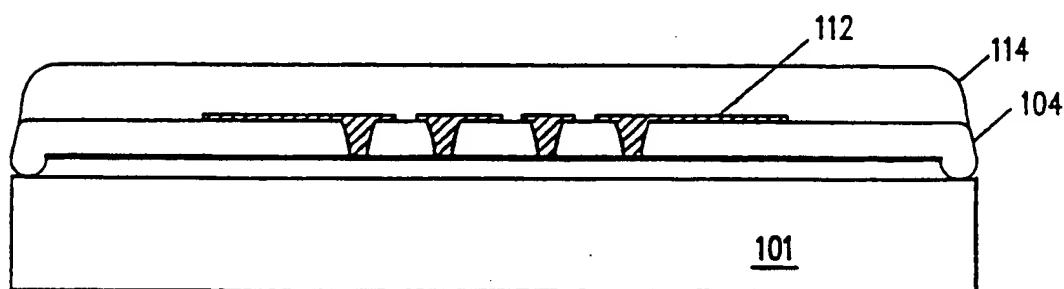


FIG. 8

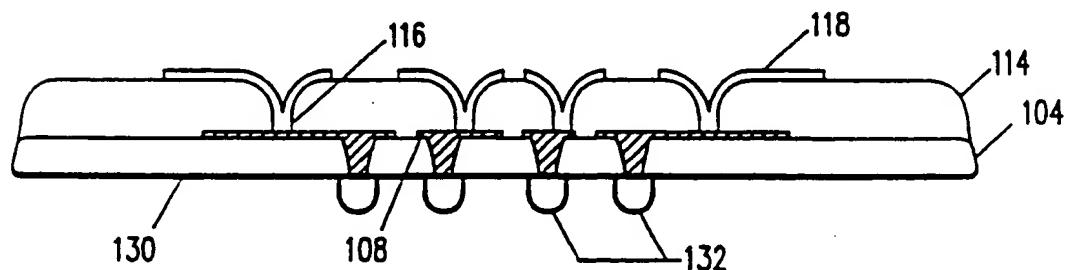


FIG. 9

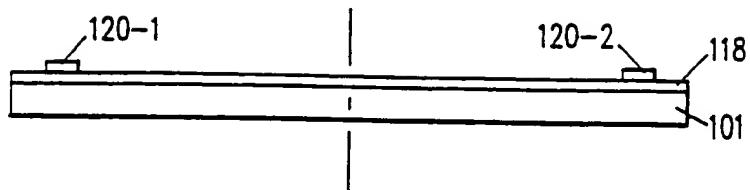


FIG. 10

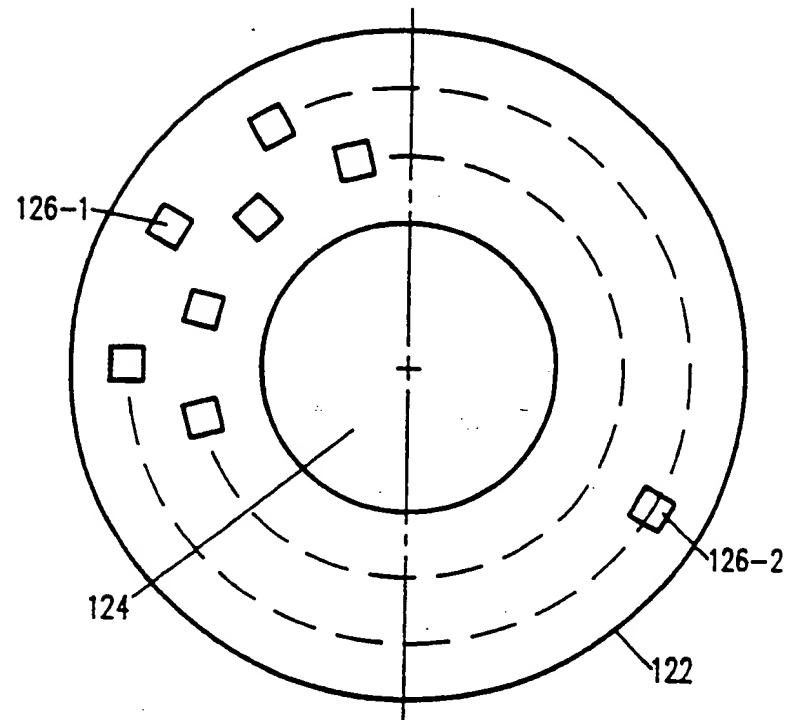


FIG. 11

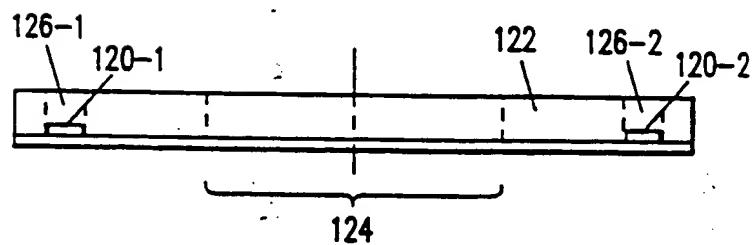


FIG. 12

**SUBSTITUTE SHEET**

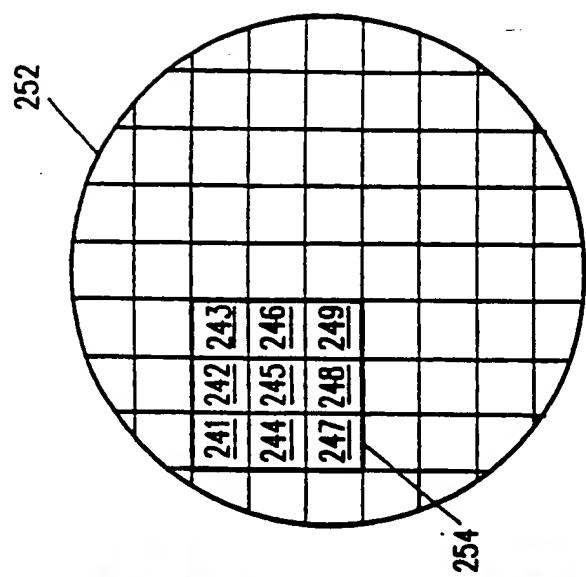


FIG. 16

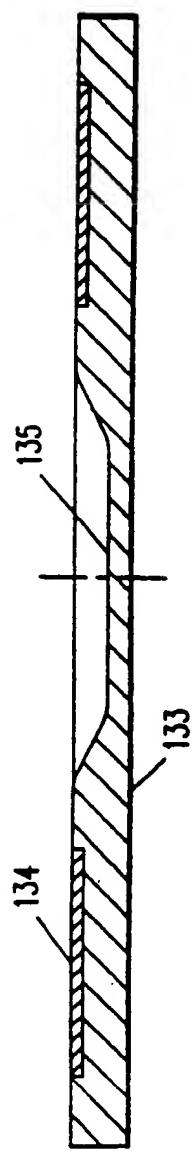


FIG. 13

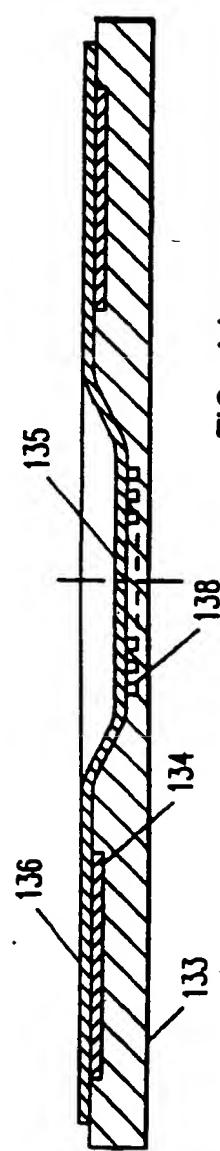


FIG. 14

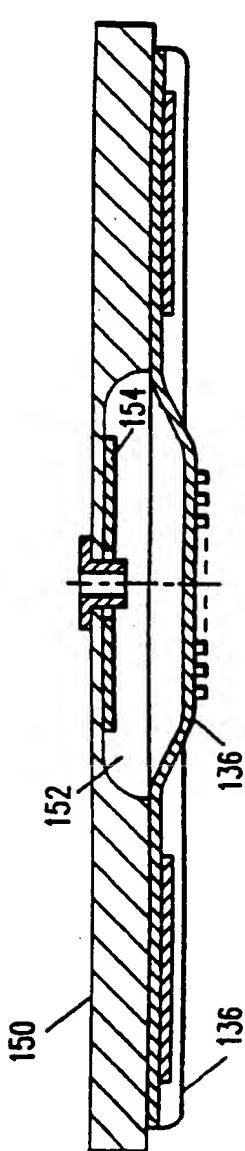


FIG. 15

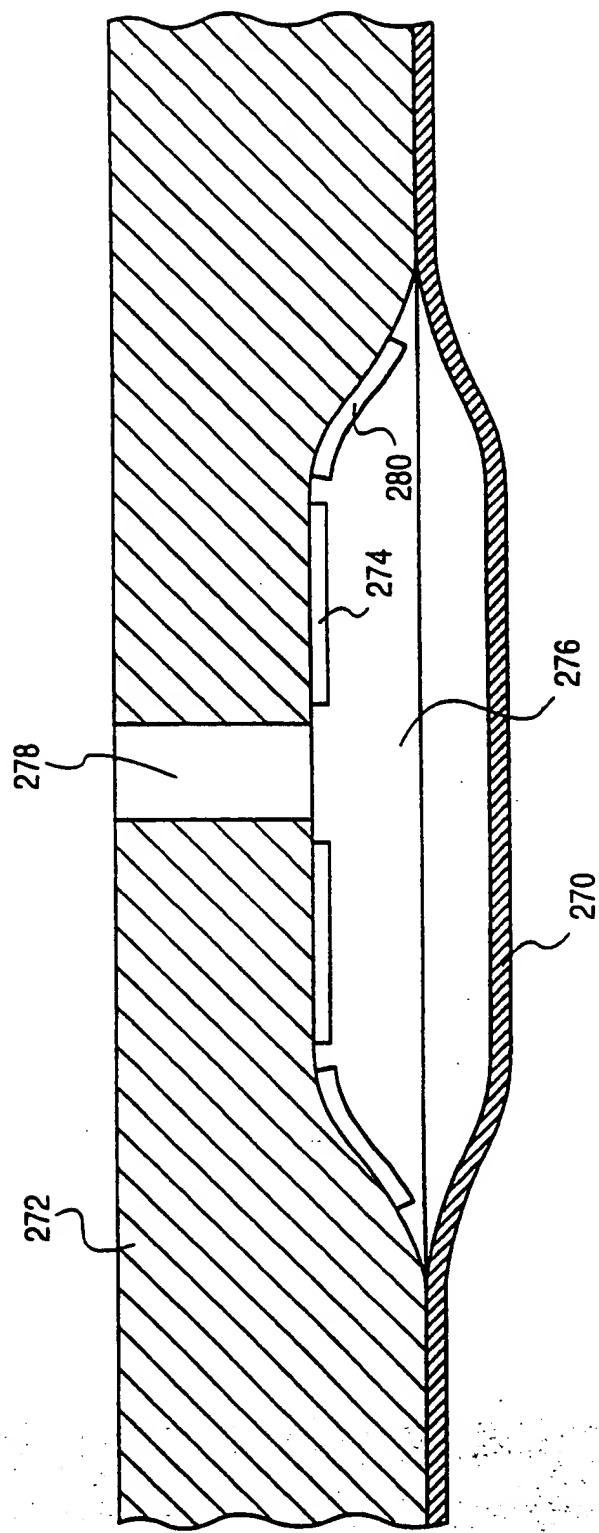


FIG. 17a

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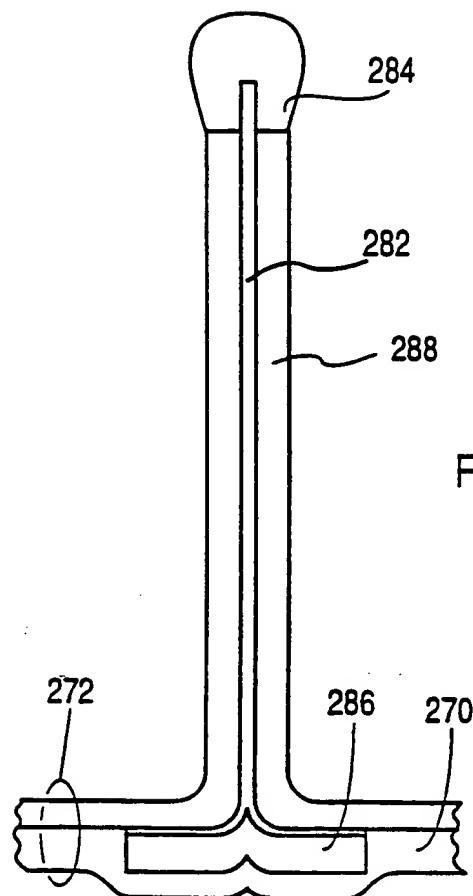
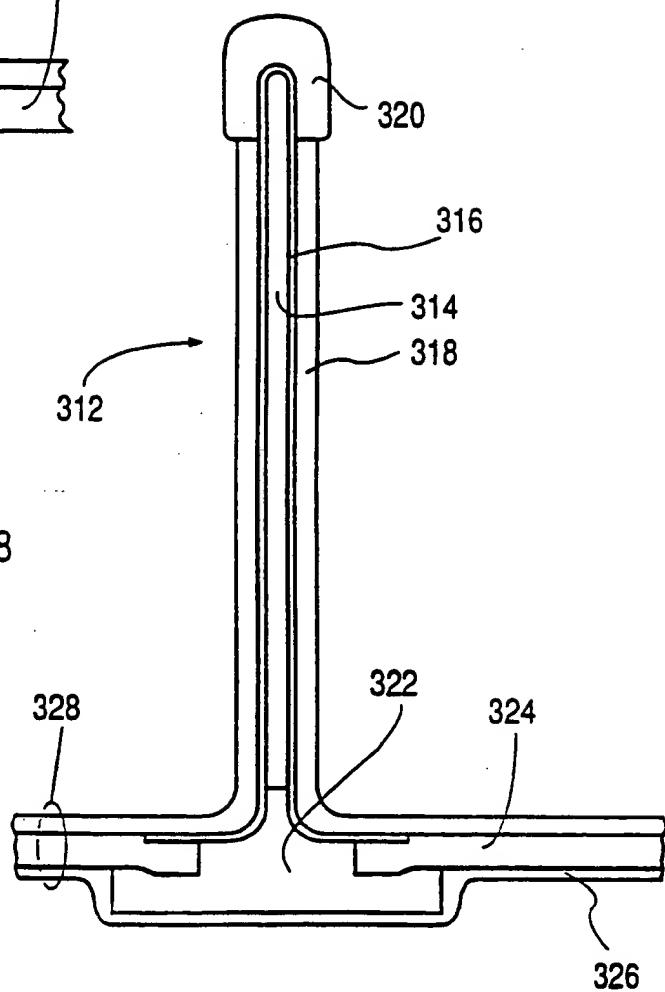


FIG. 18



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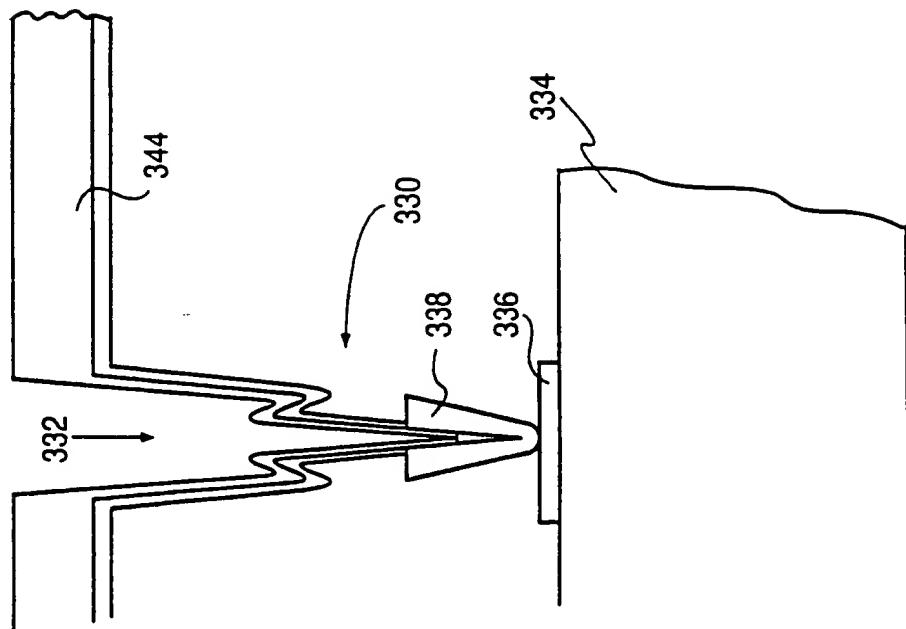


FIG. 19b

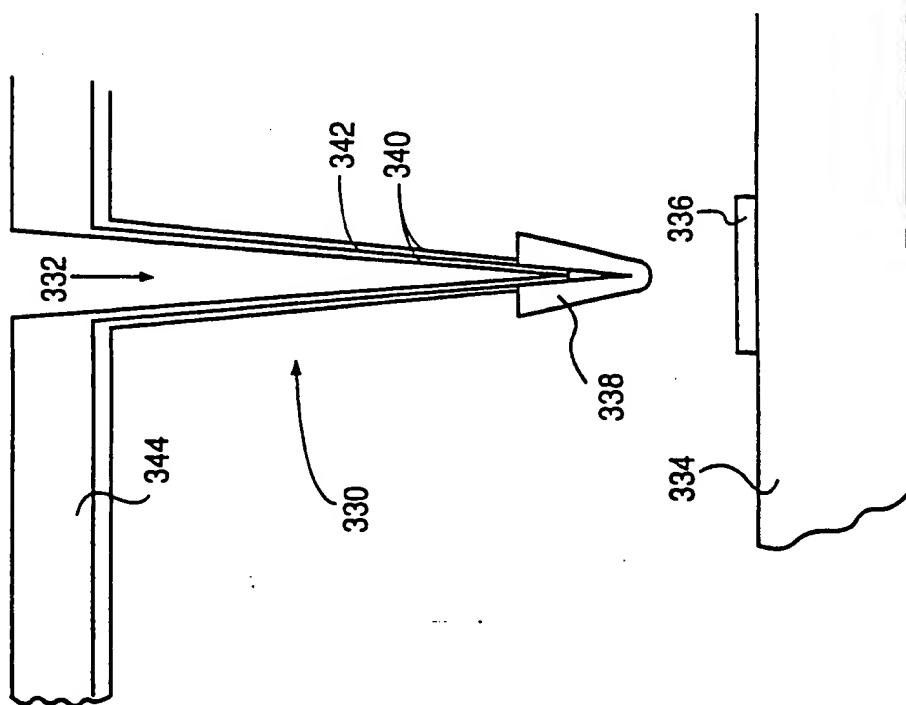


FIG. 19a

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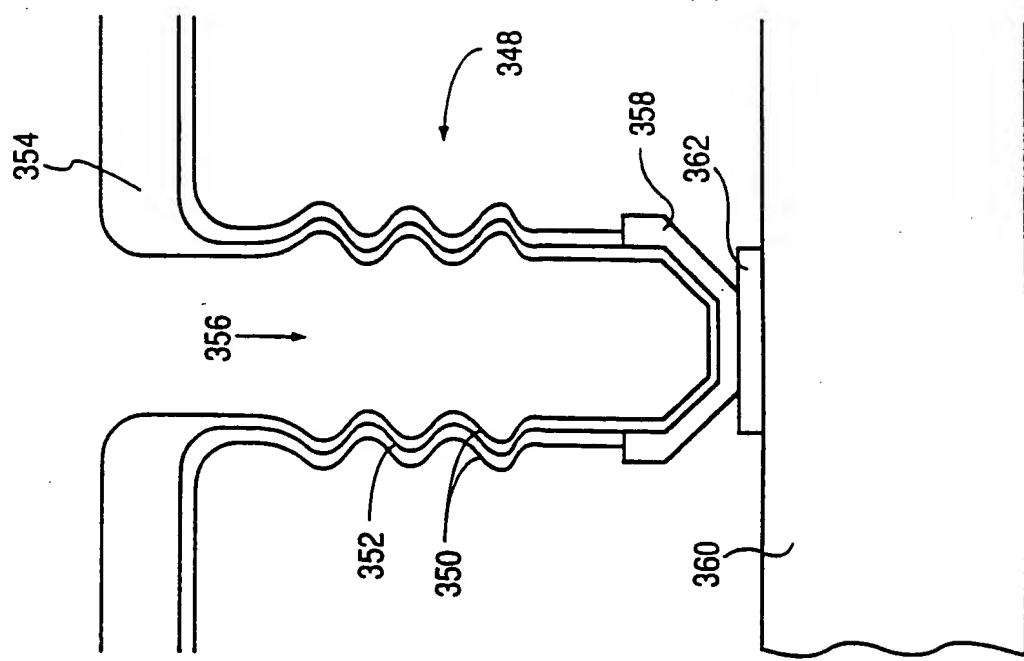


FIG. 20b

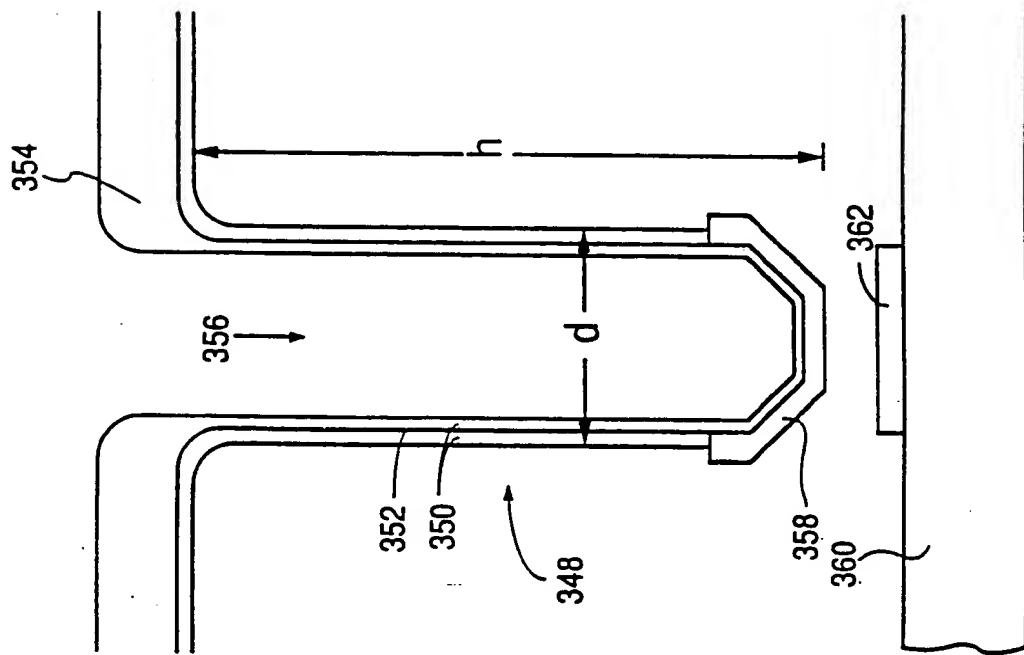


FIG. 20a

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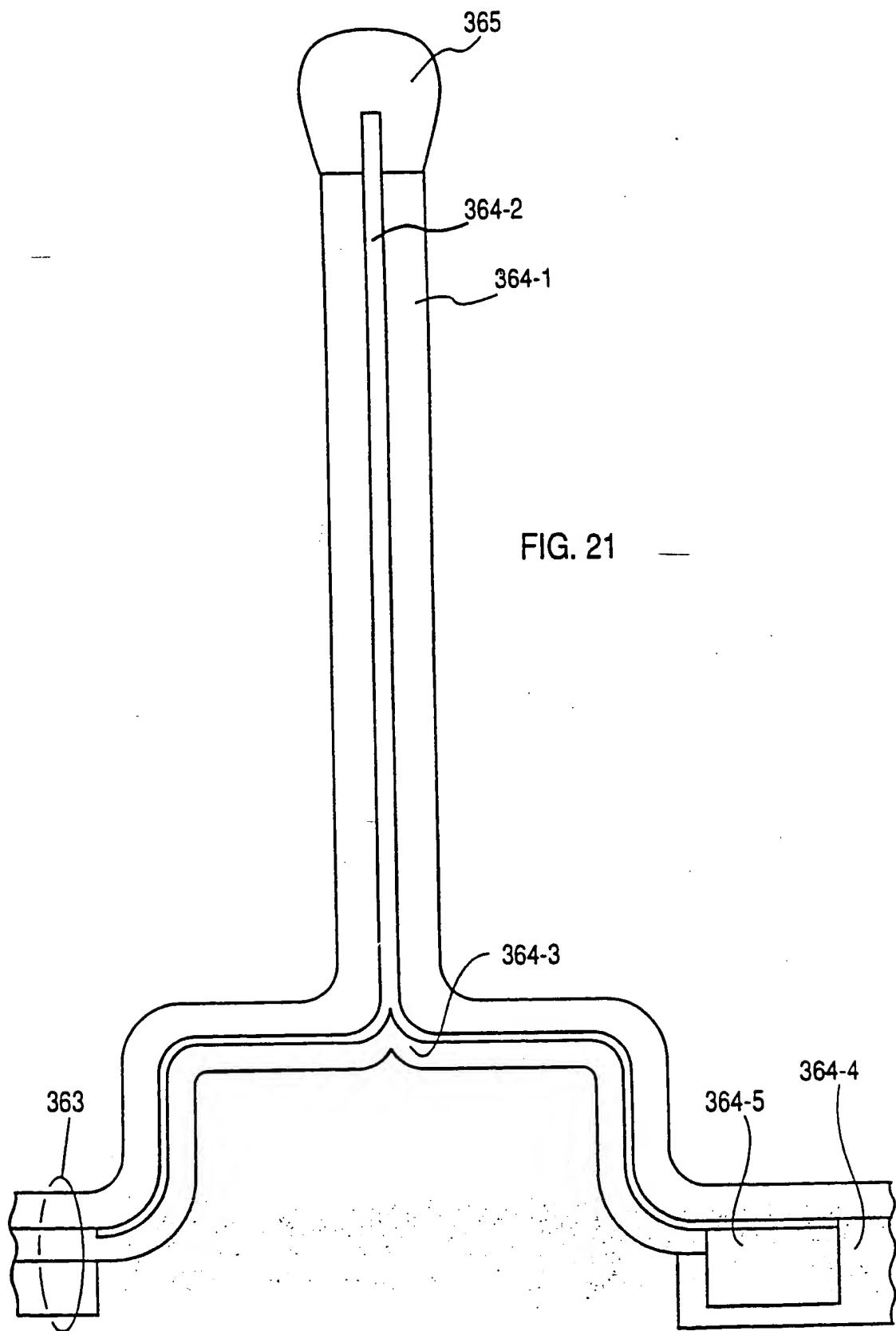


FIG. 21

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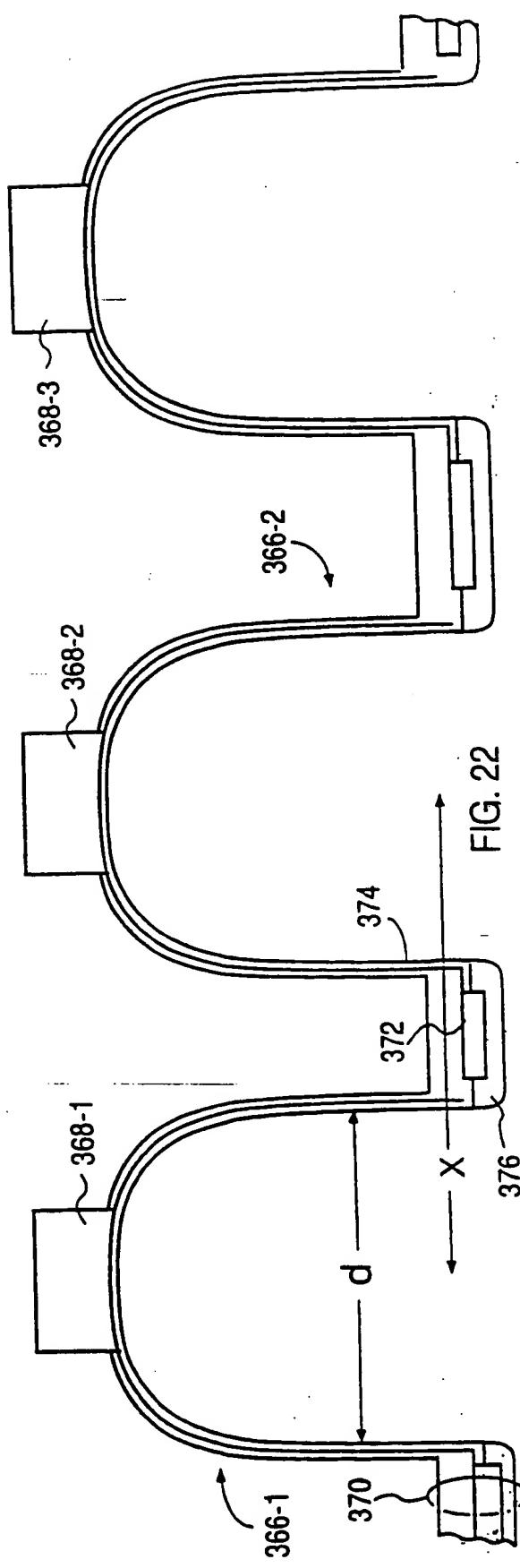


FIG. 22

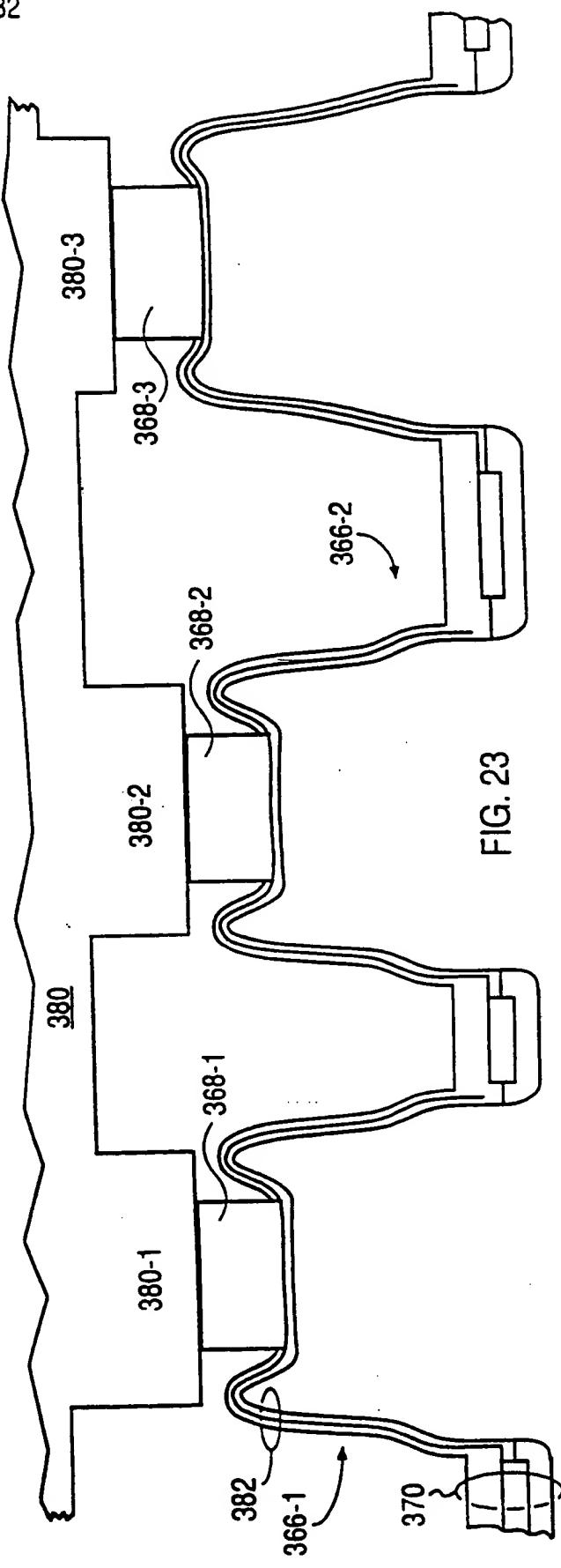
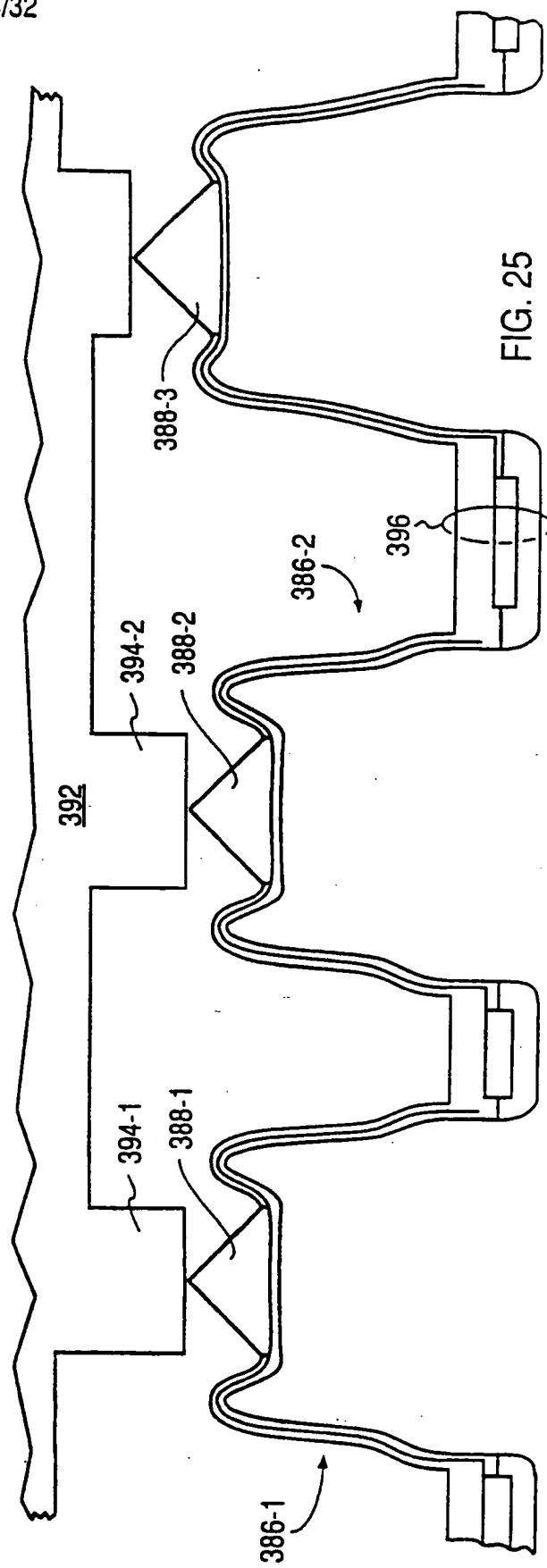
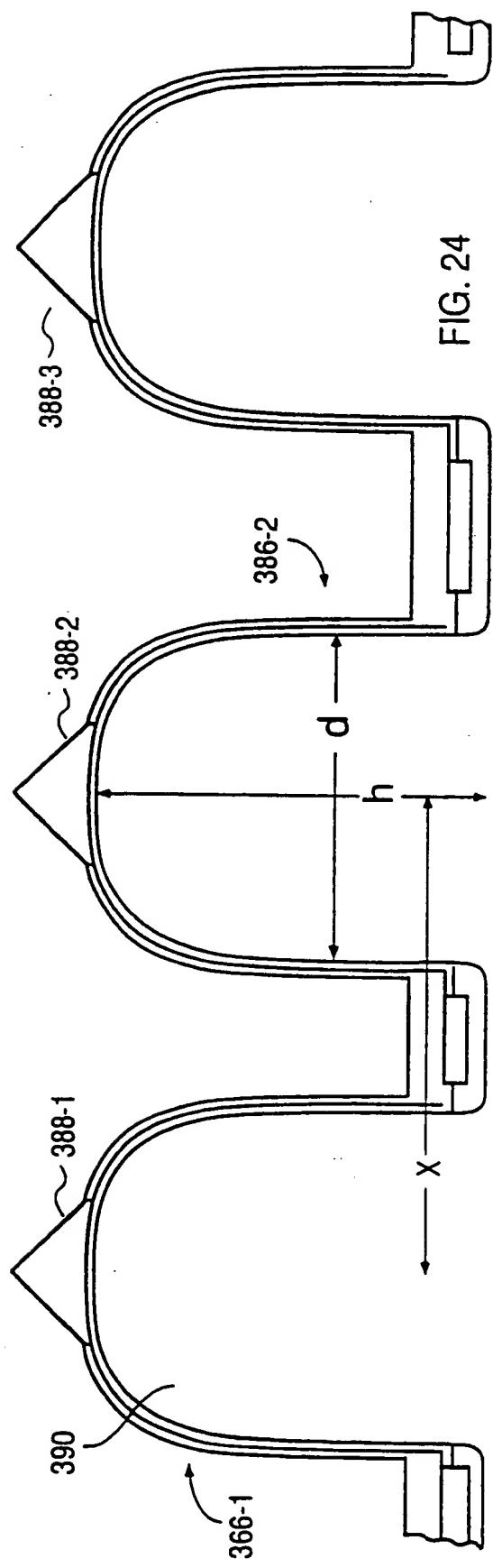


FIG. 23

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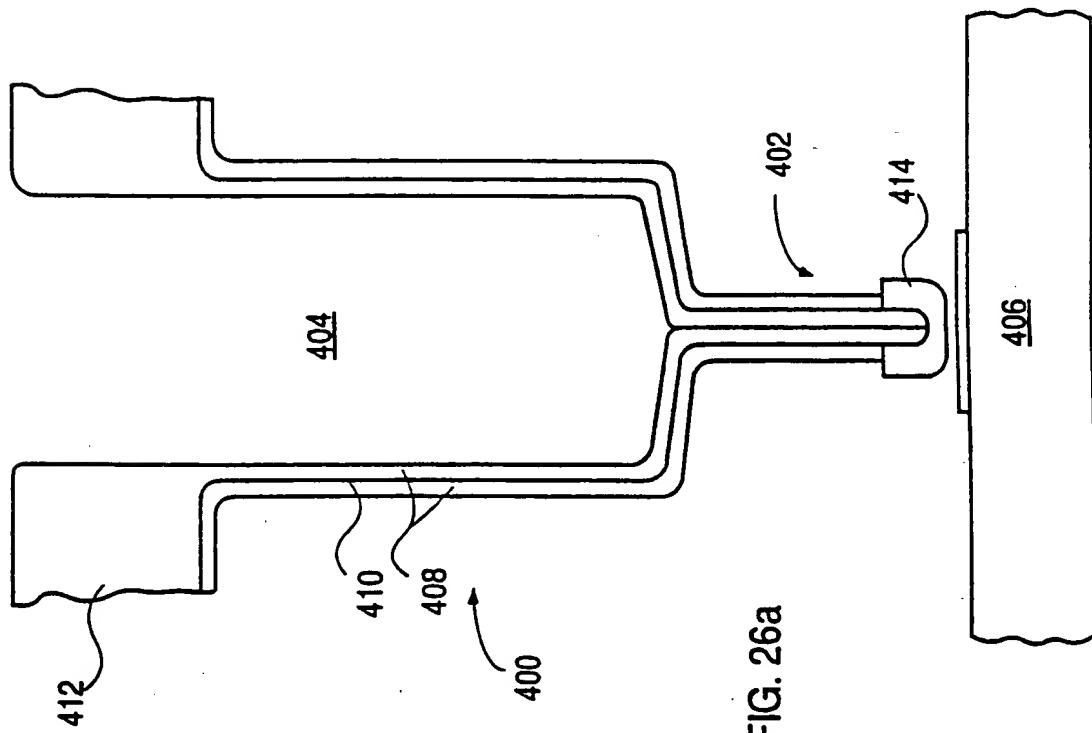
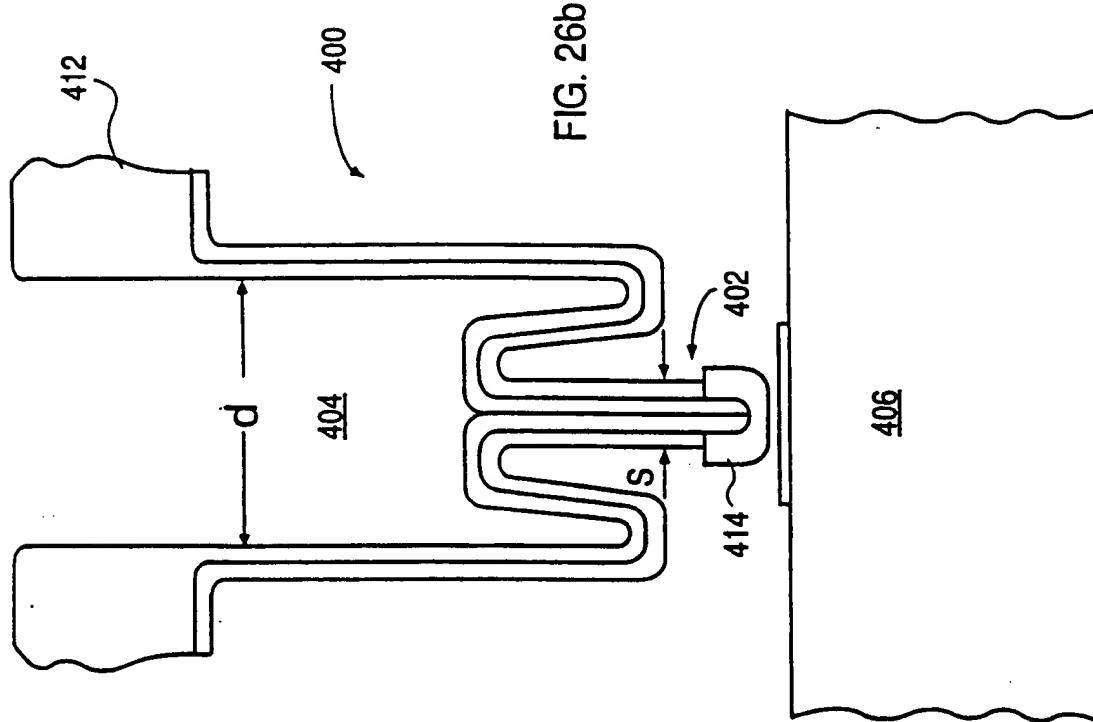
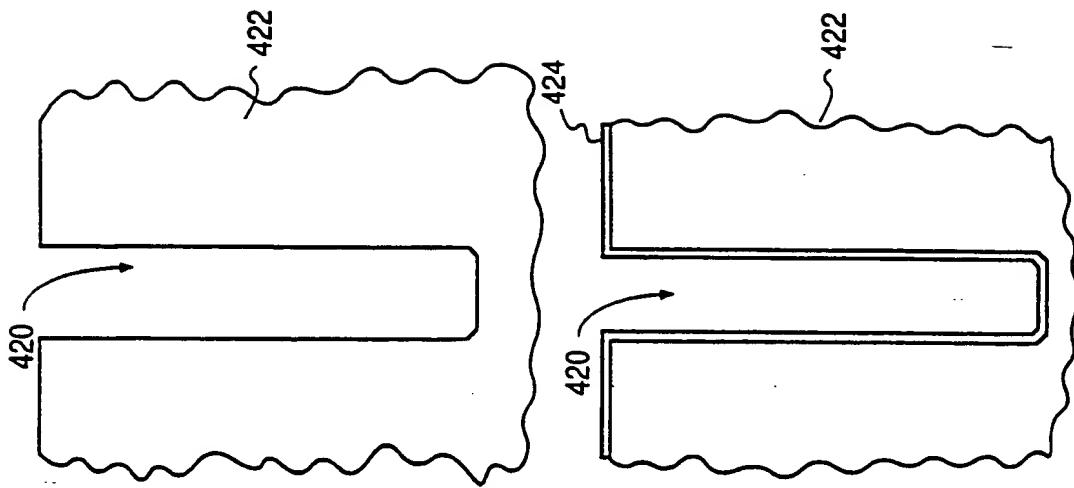


FIG. 28a



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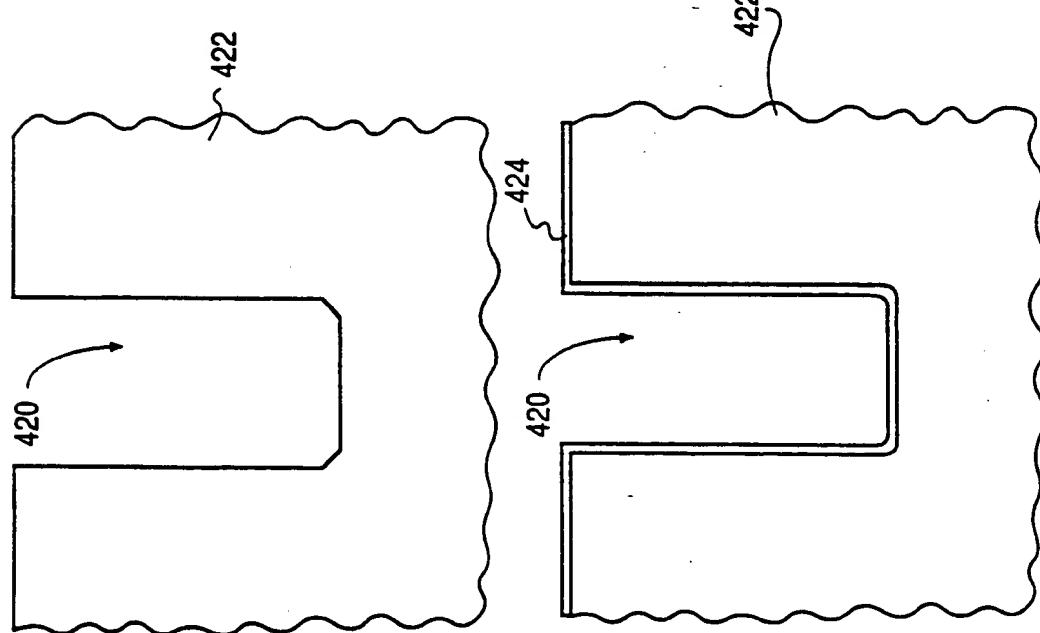


FIG. 27b

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FIG. 28c

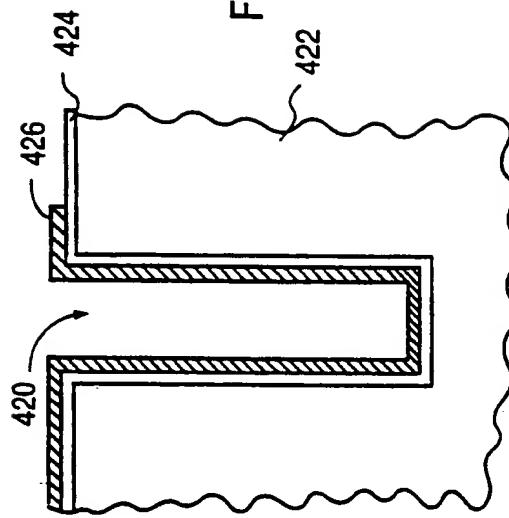
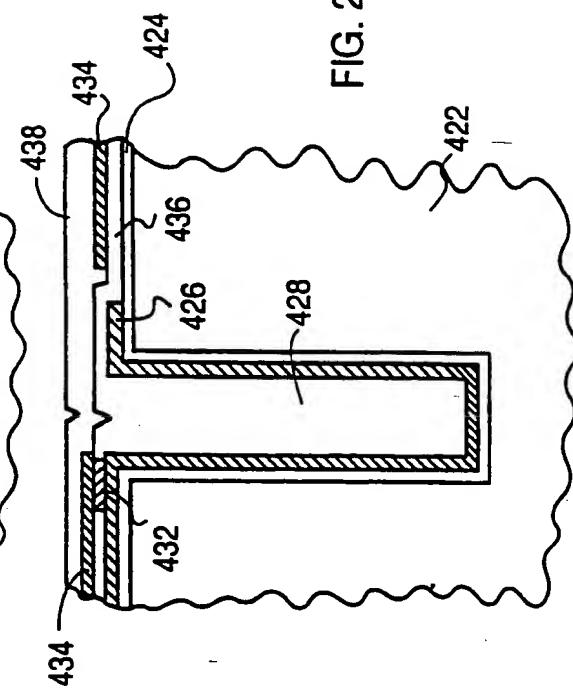


FIG. 28d



422

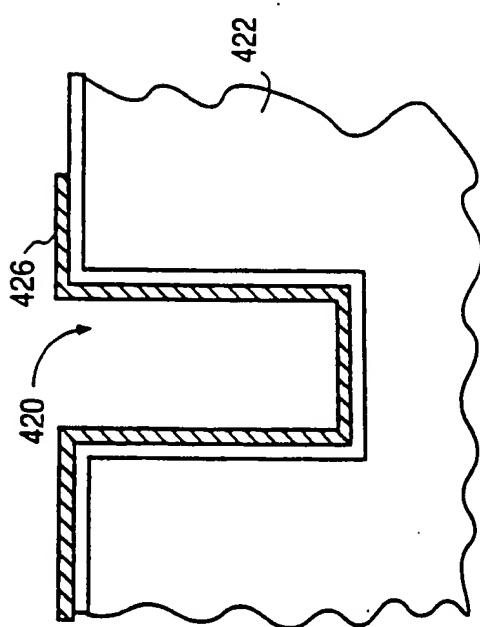


FIG. 27c

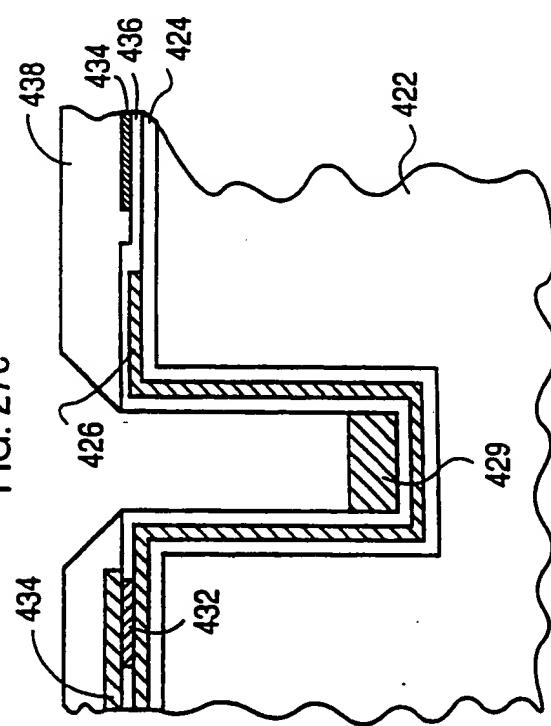
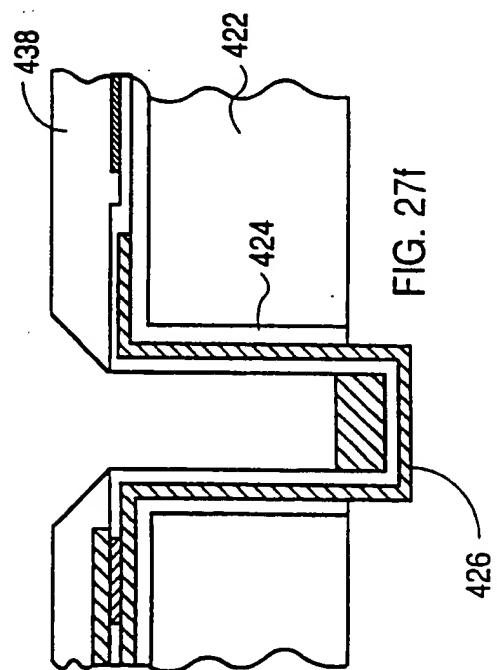
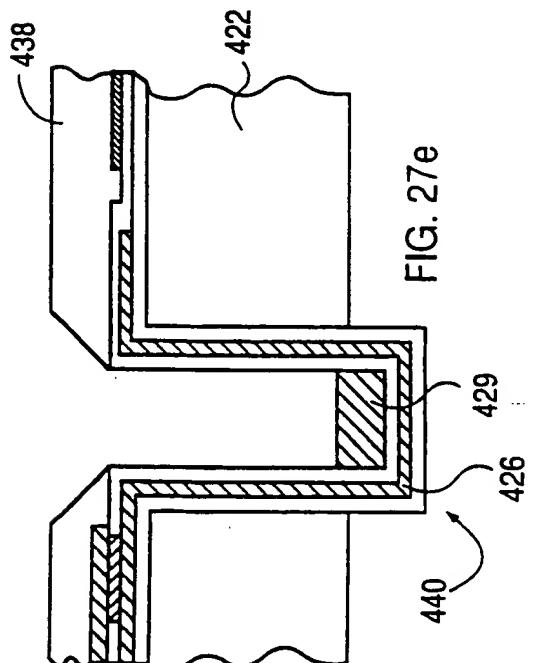
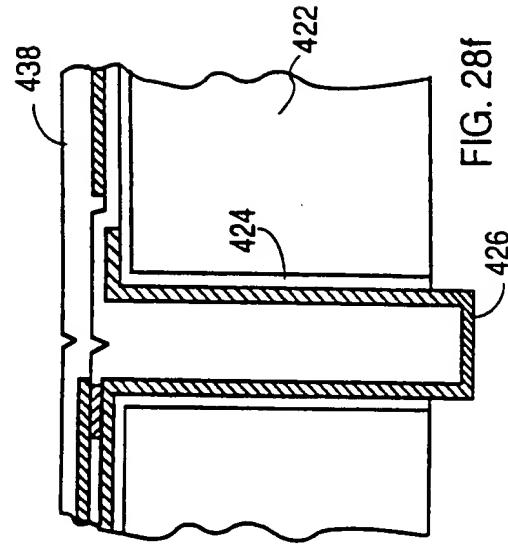
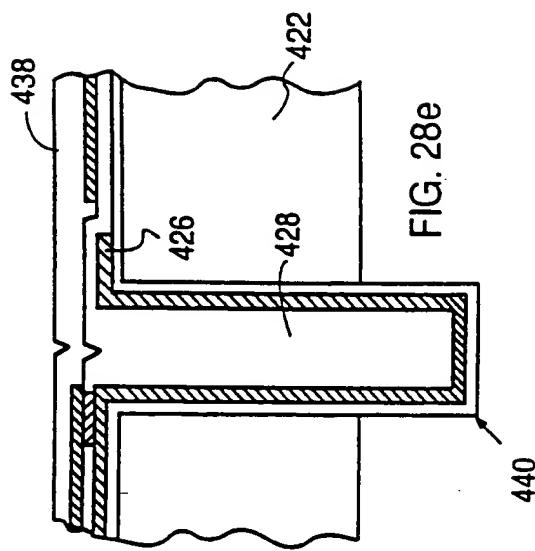


FIG. 27d



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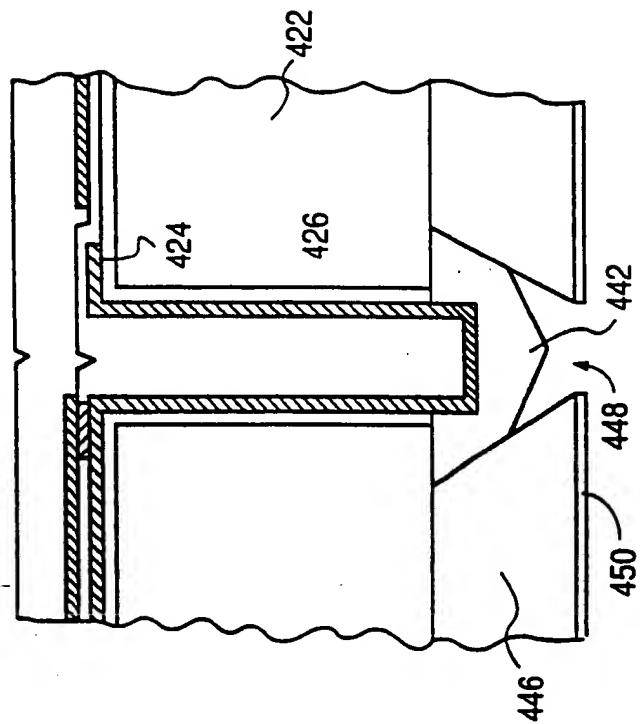


FIG. 28g

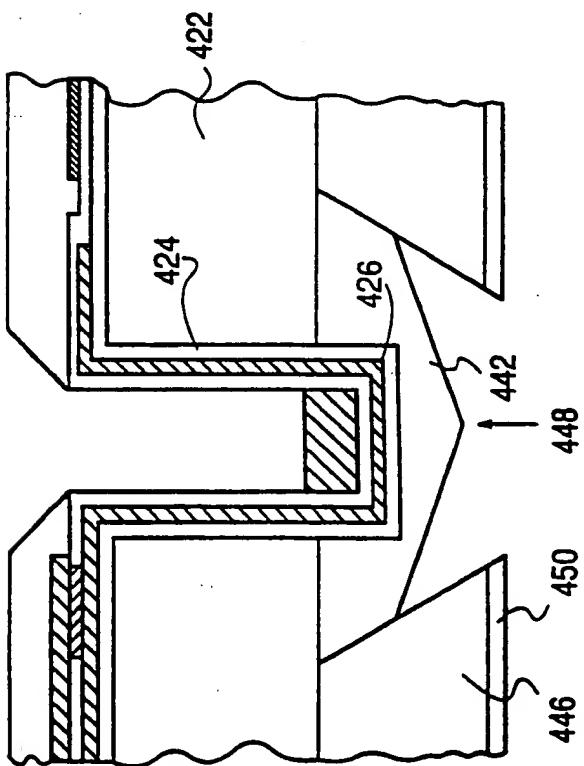


FIG. 27g

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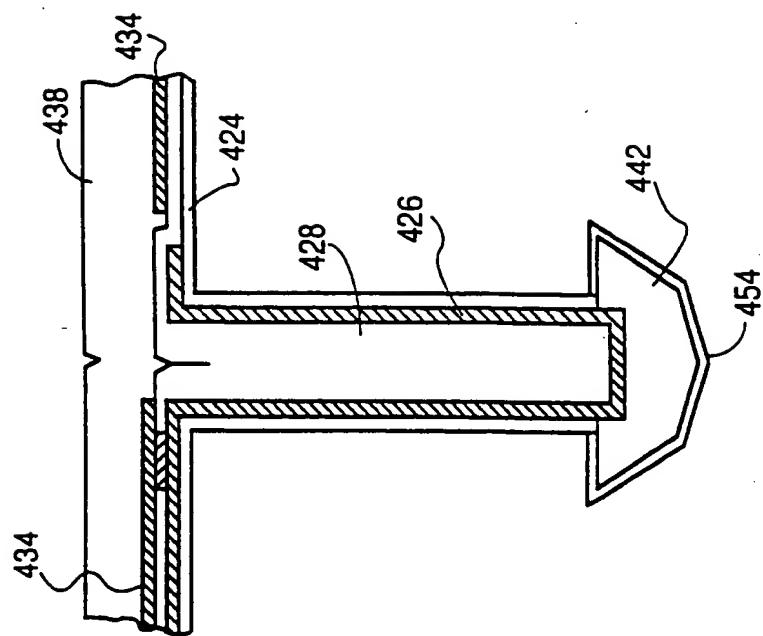


FIG. 28h

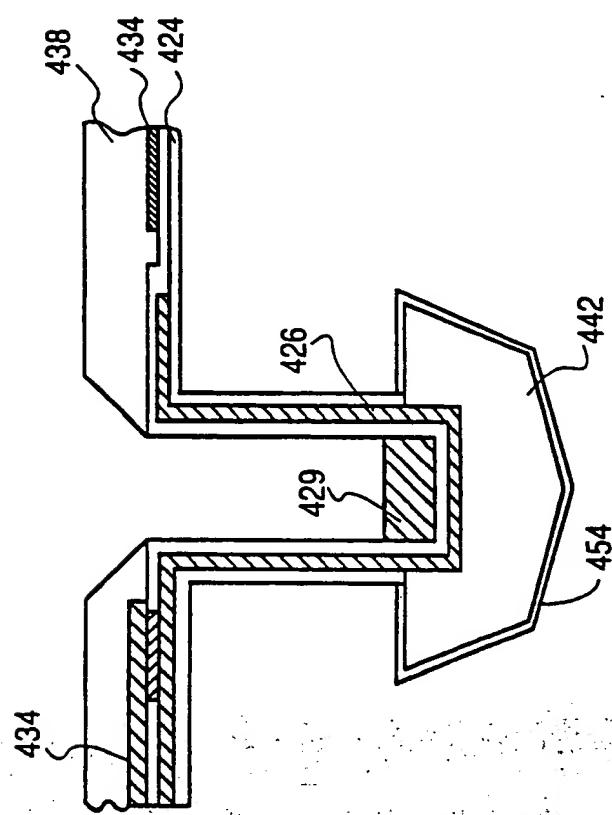


FIG. 27h

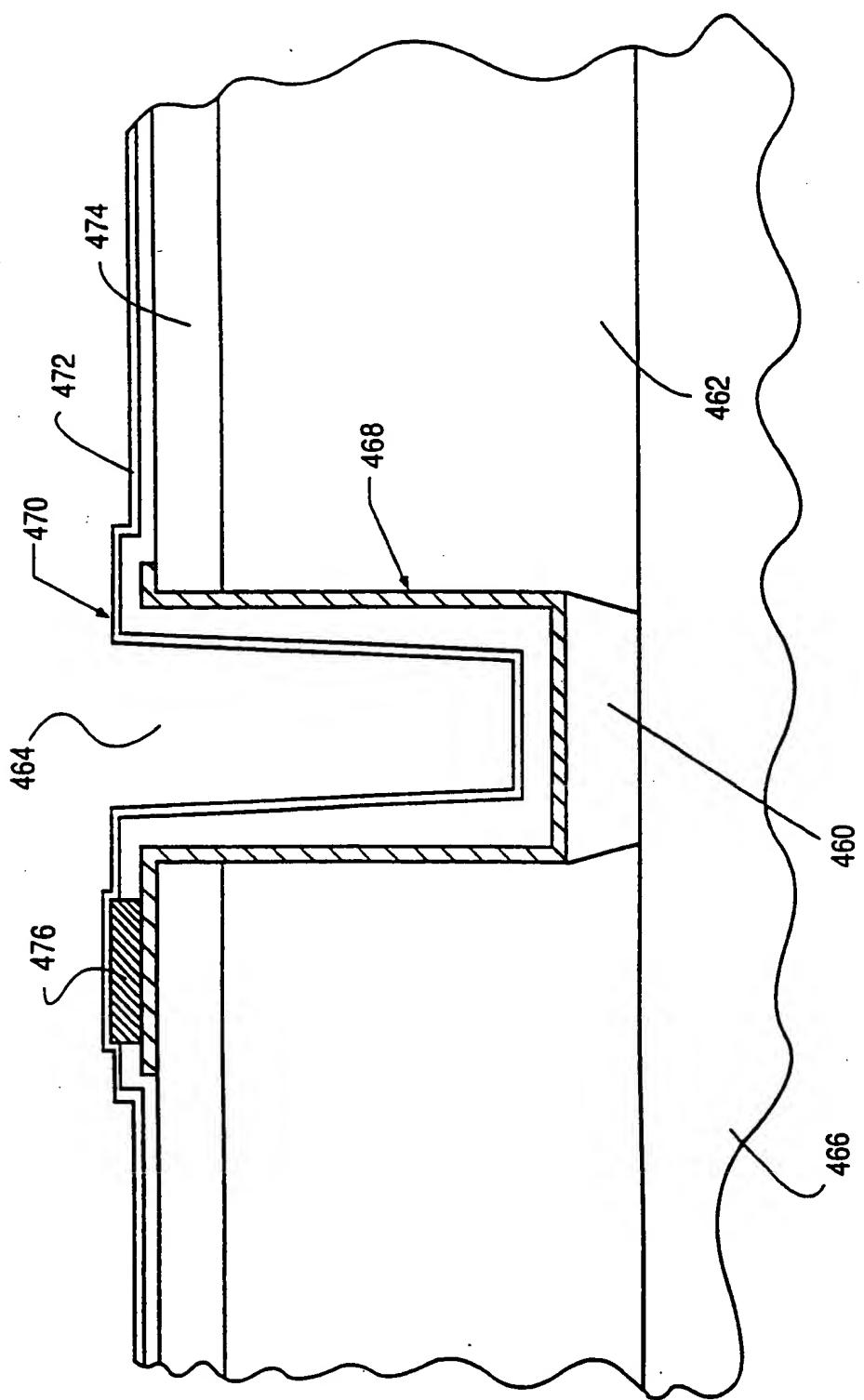


FIG. 29

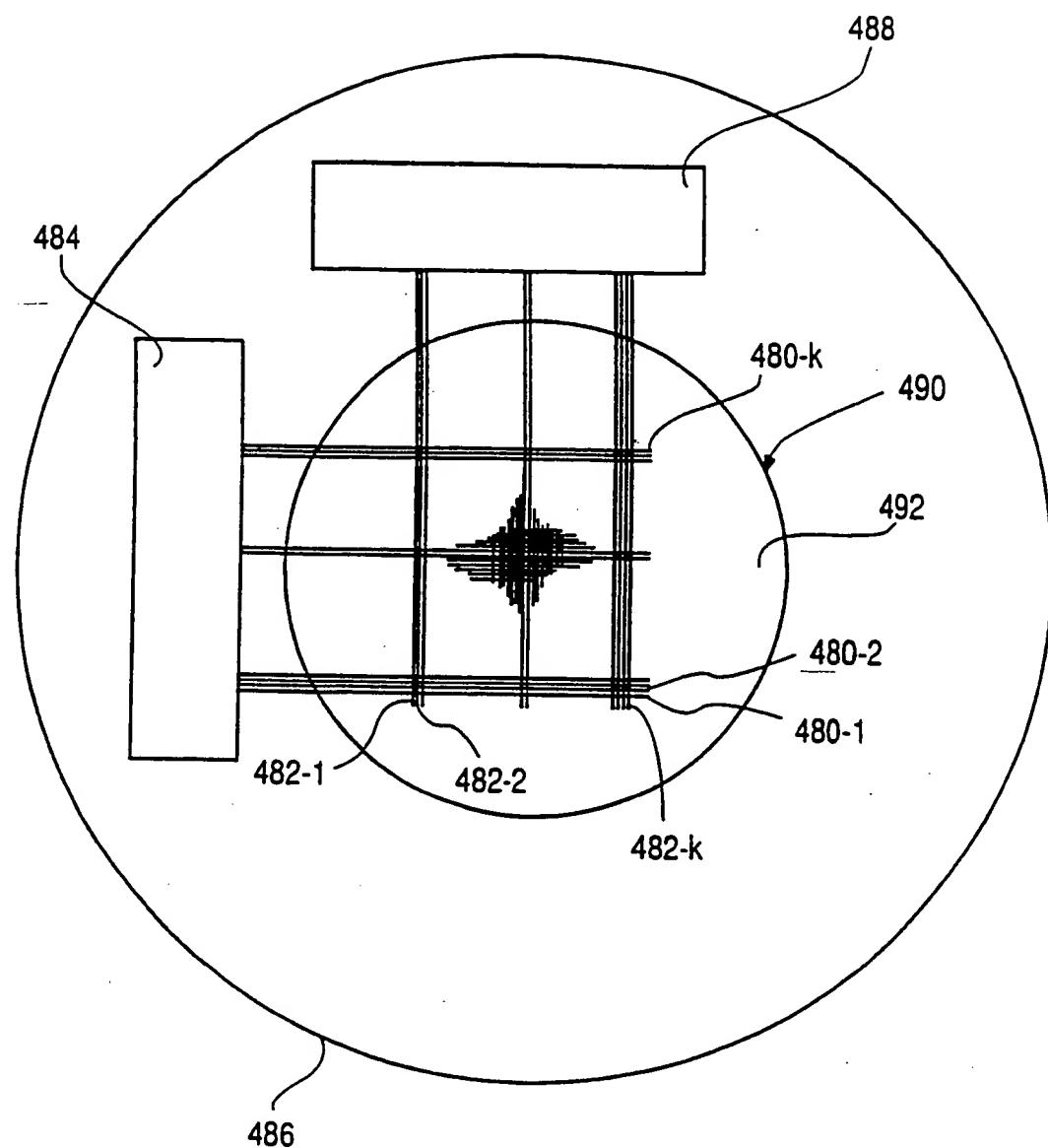


FIG. 30

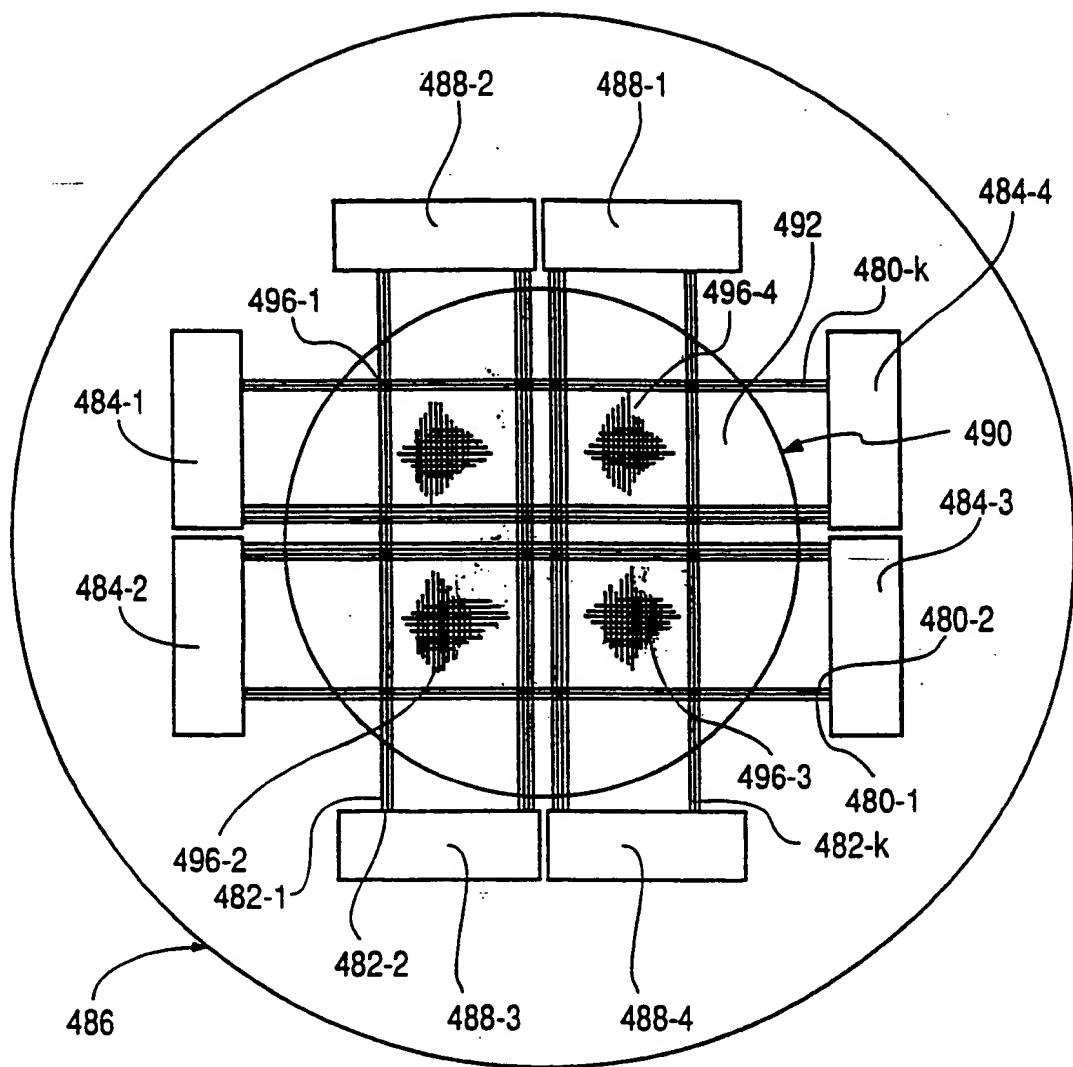
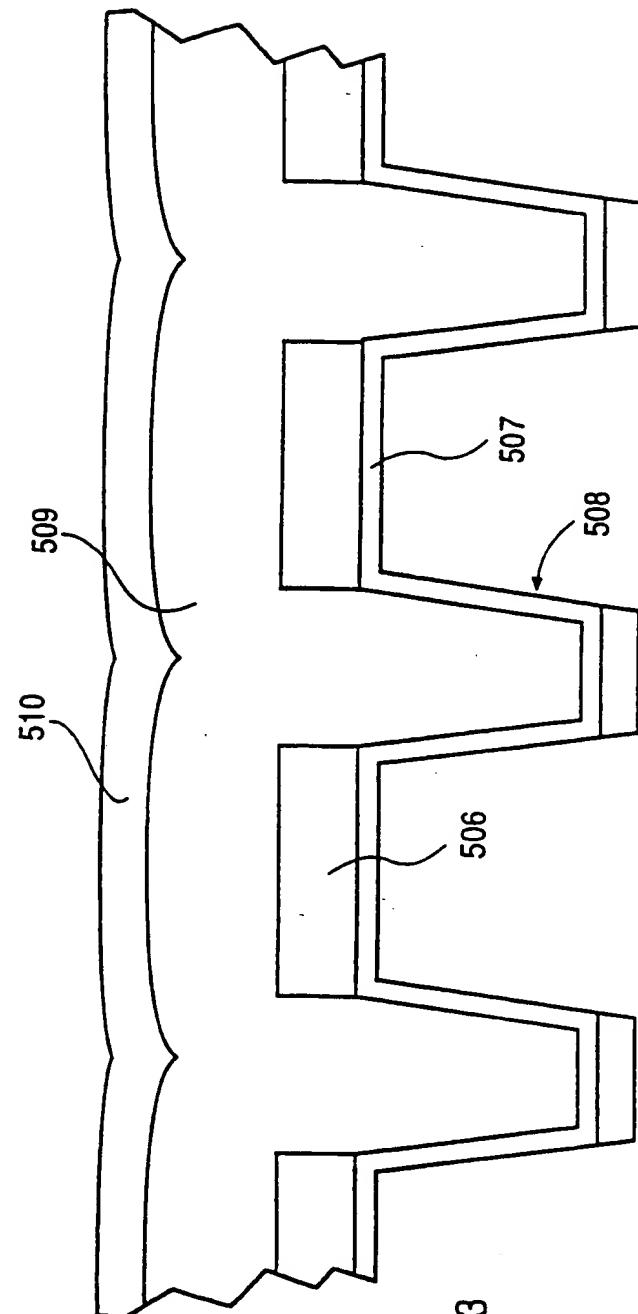
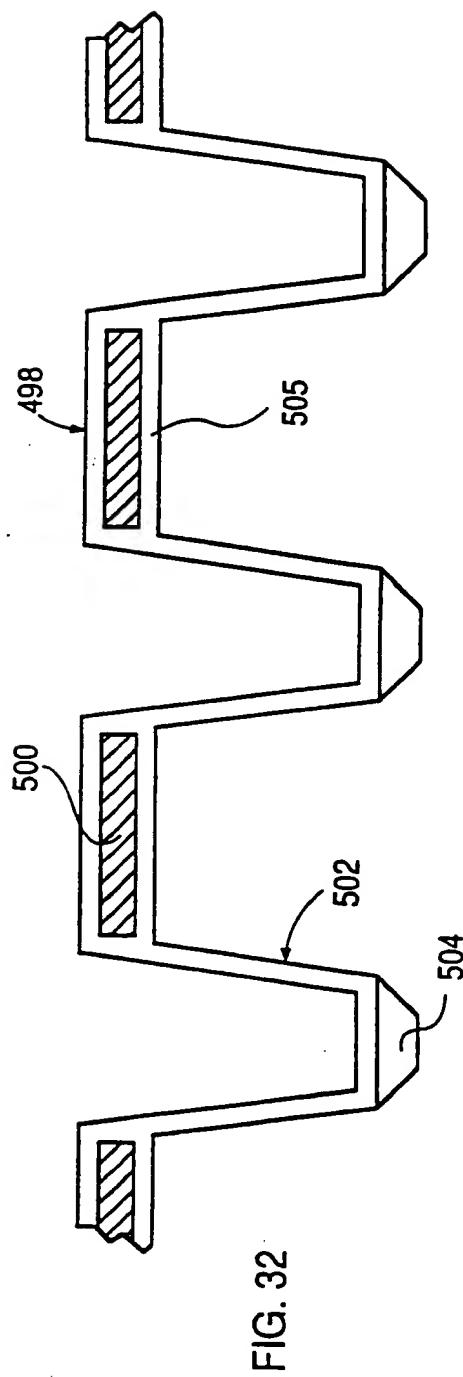


FIG. 31



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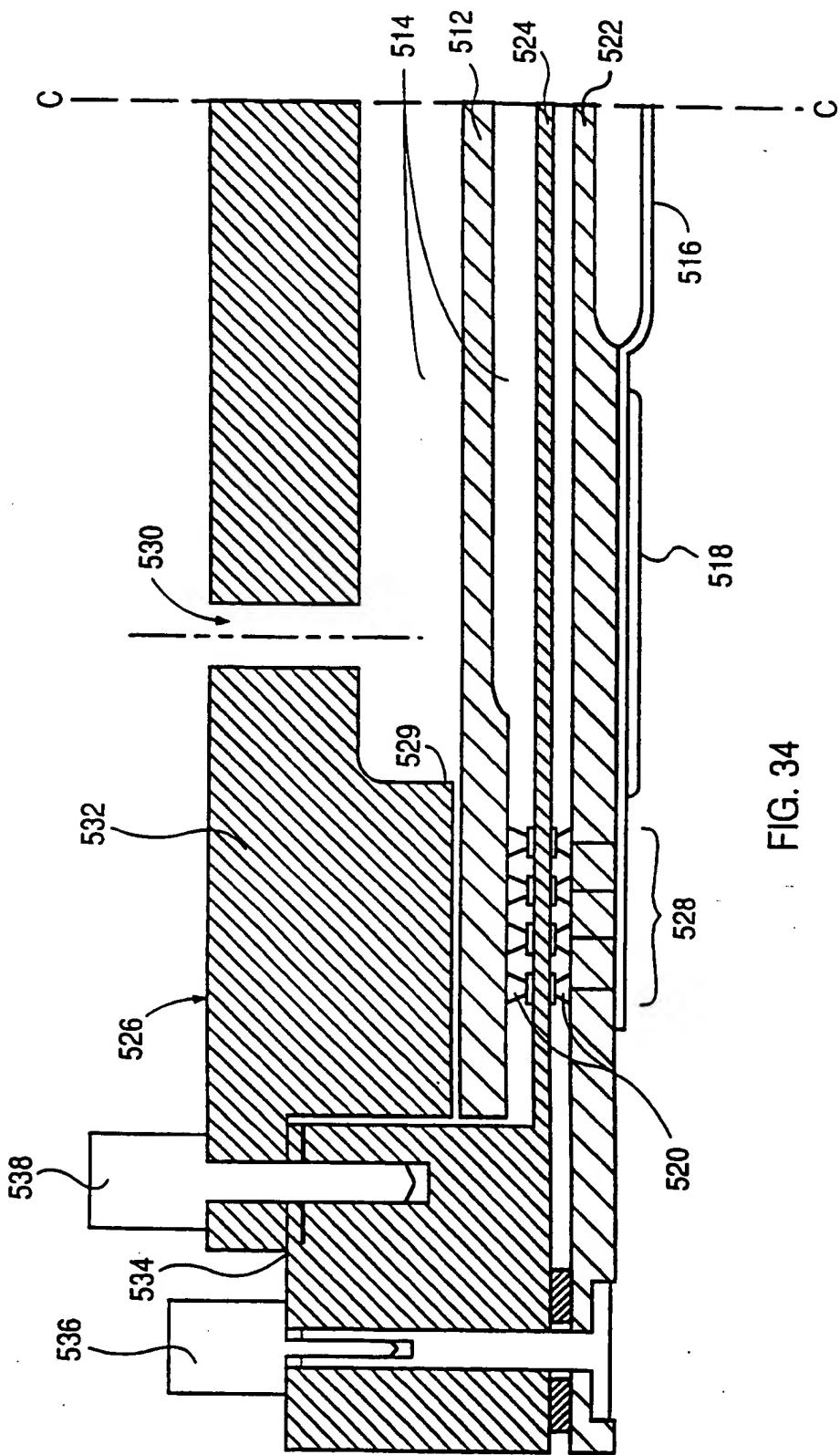


FIG. 34

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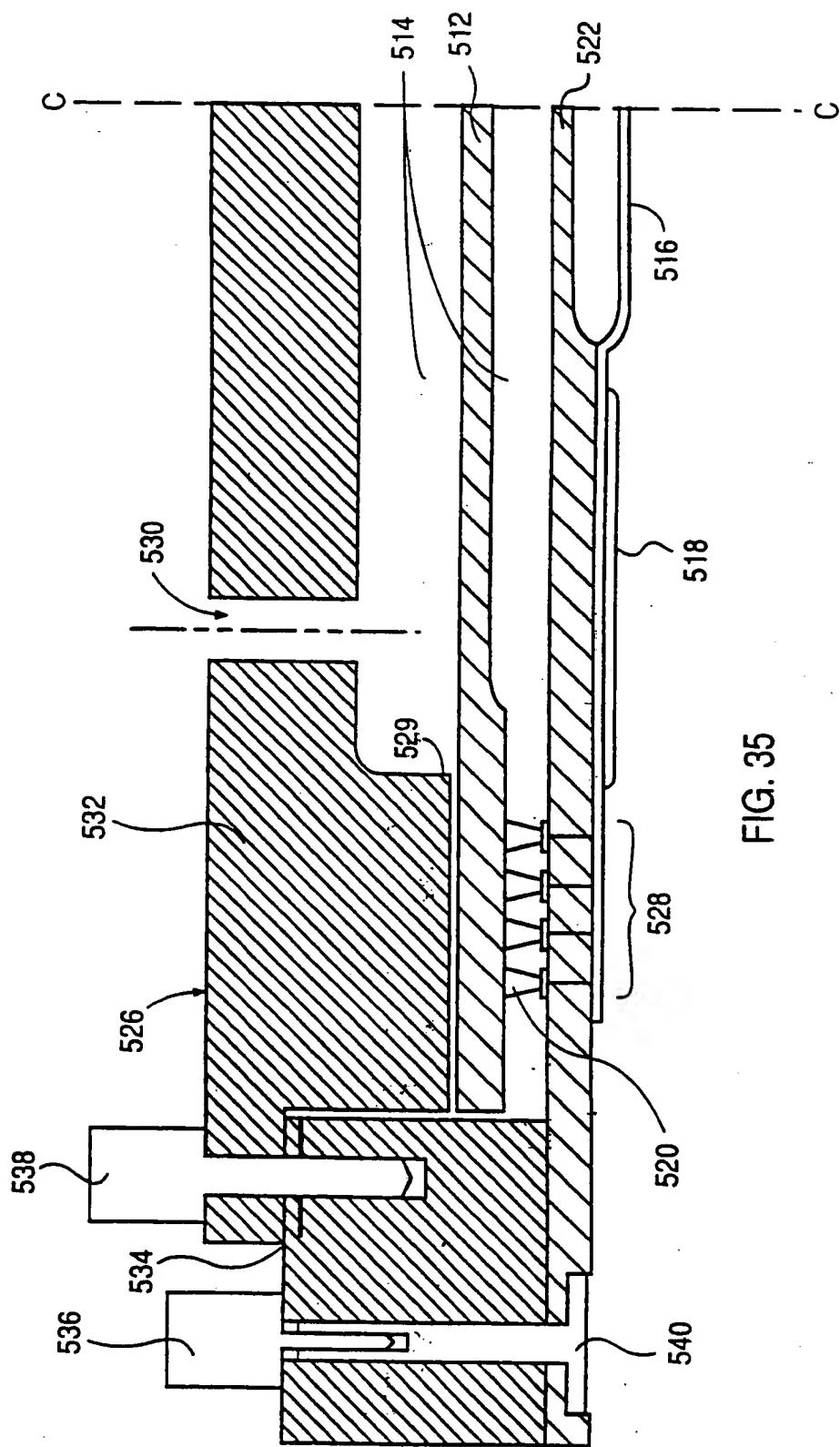


FIG. 35

SUBSTITUTE SHEET

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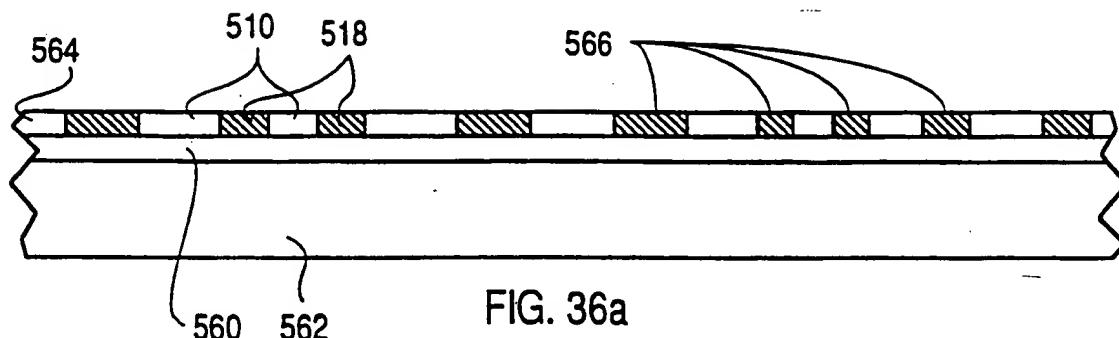


FIG. 36a

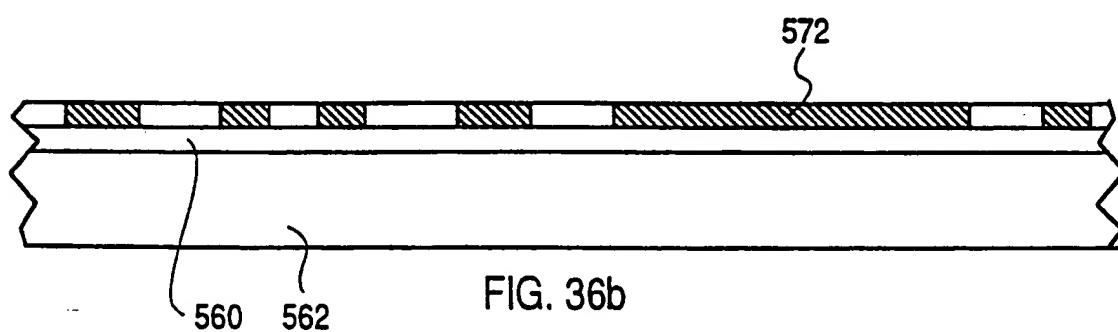


FIG. 36b

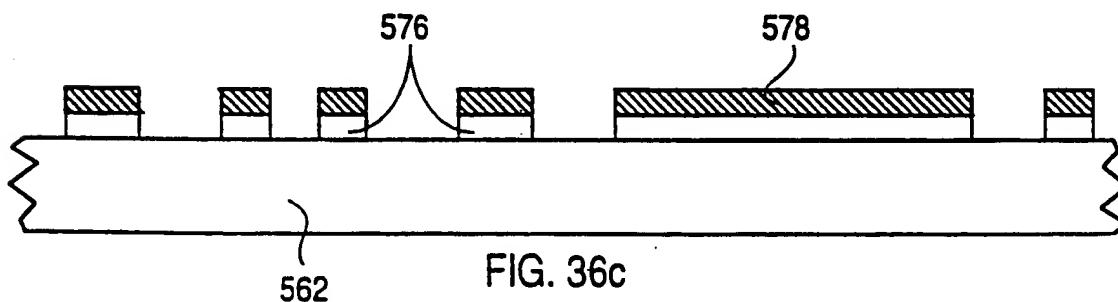


FIG. 36c

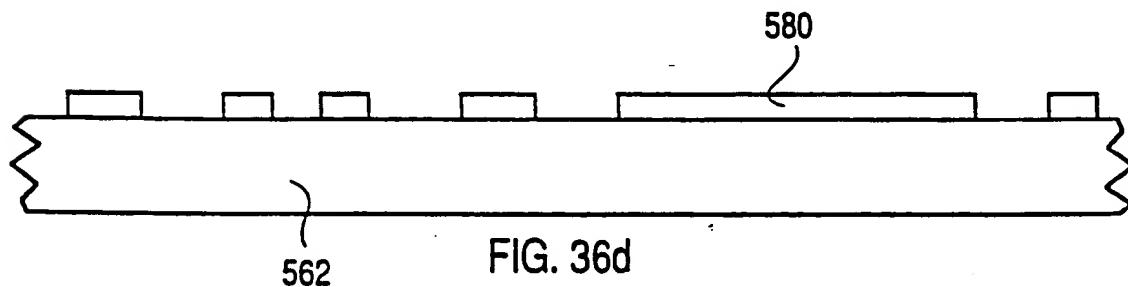


FIG. 36d

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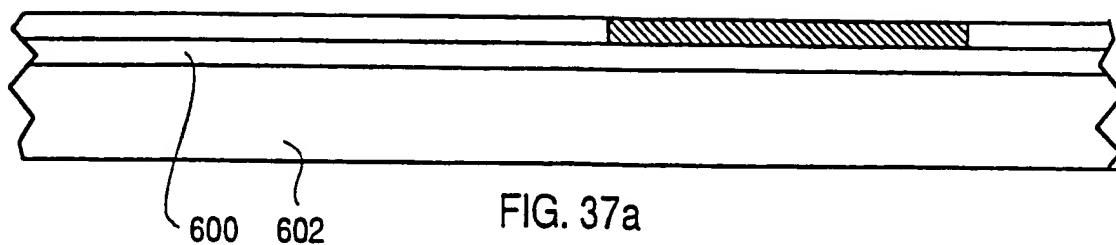


FIG. 37a

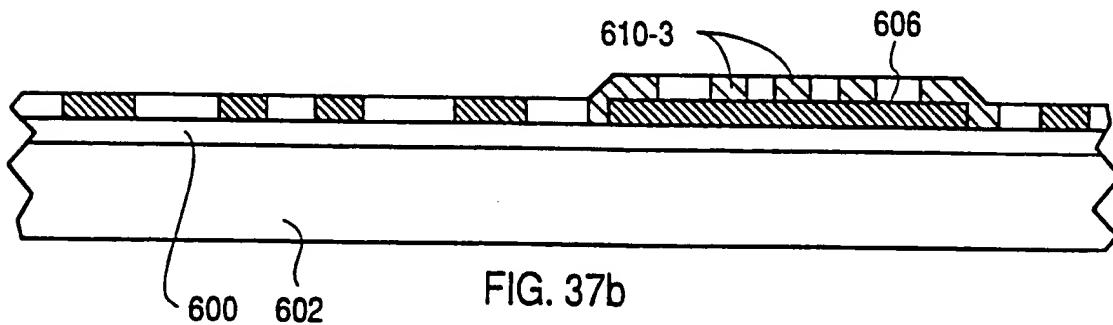


FIG. 37b

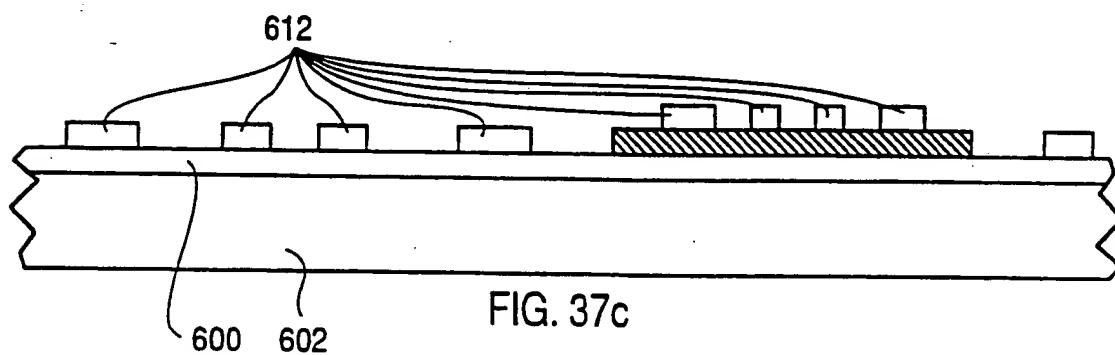


FIG. 37c

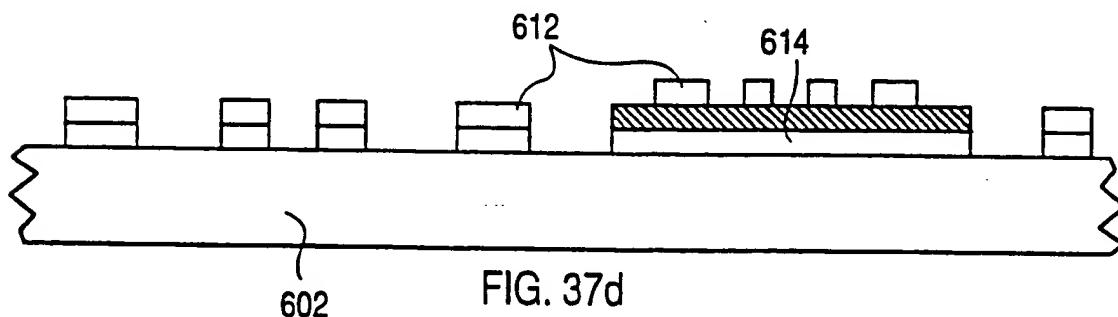


FIG. 37d

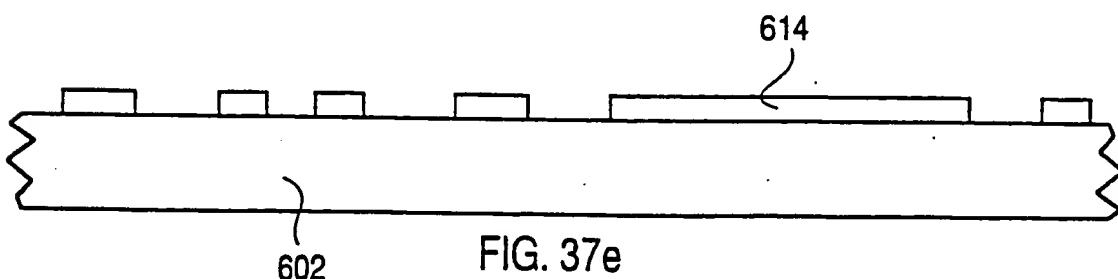
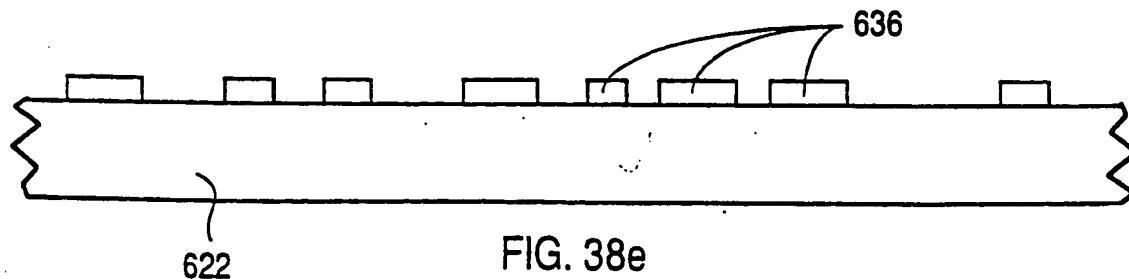
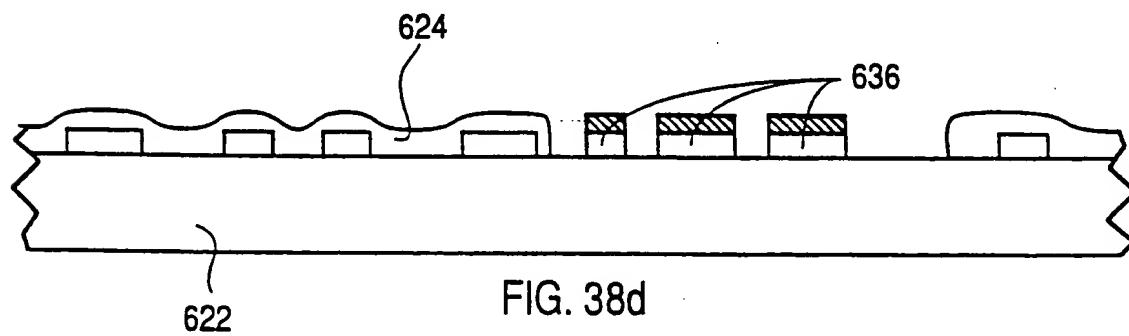
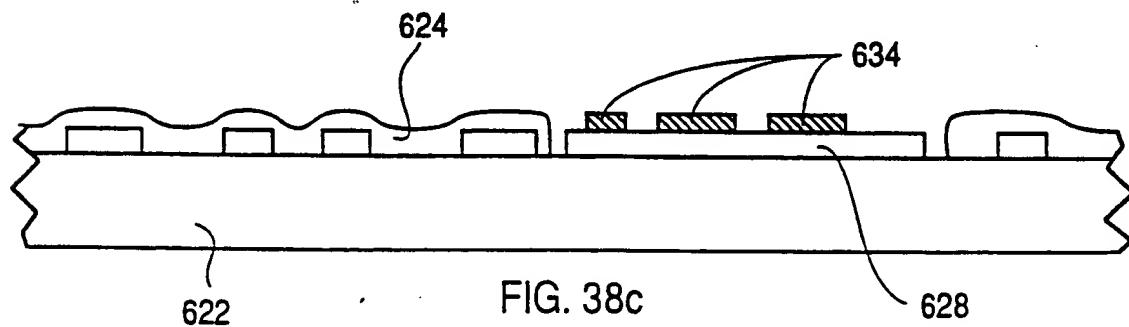
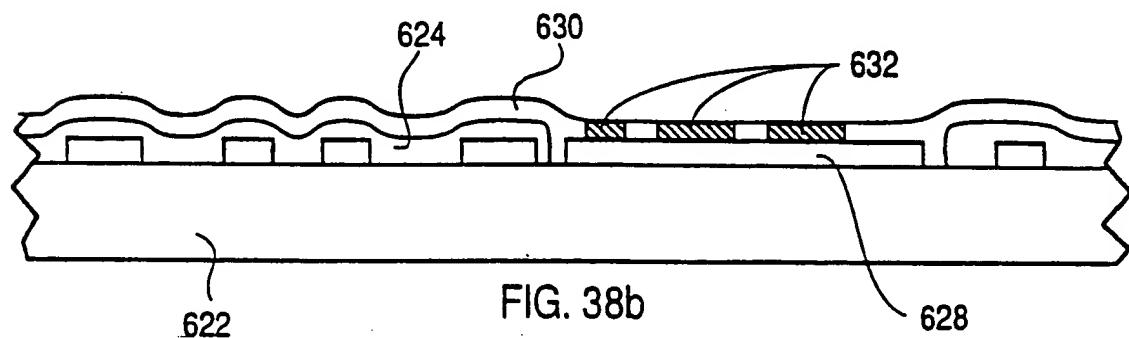
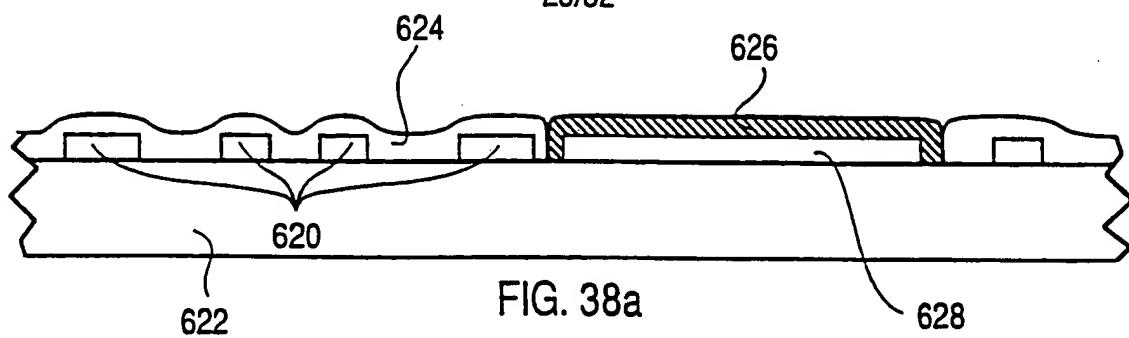


FIG. 37e

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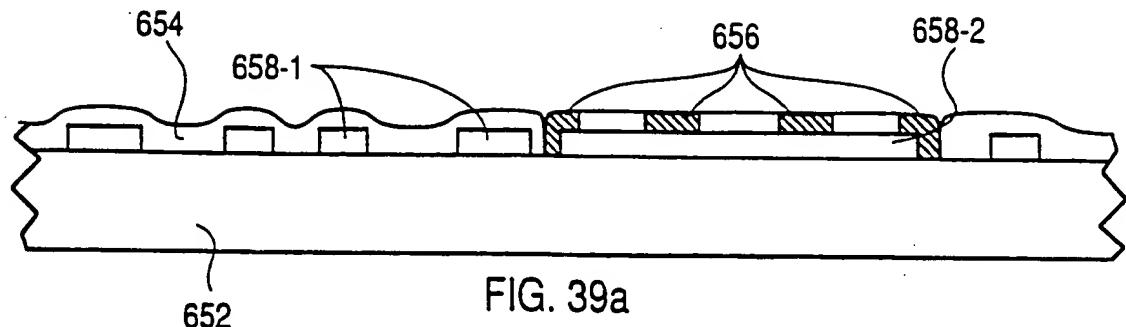


FIG. 39a

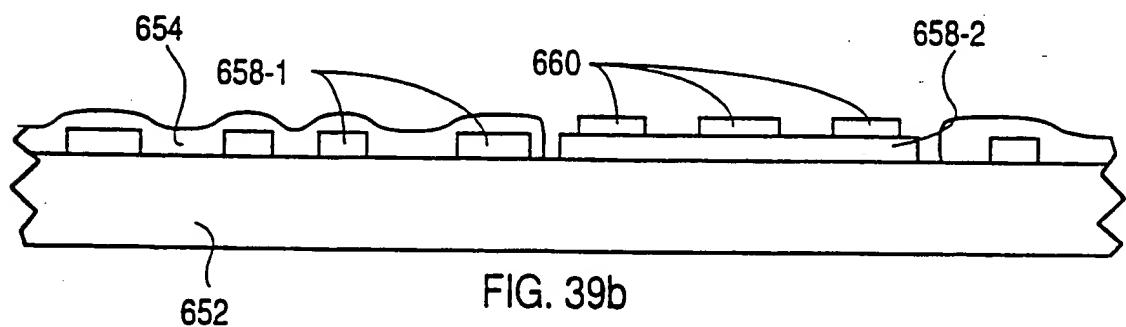


FIG. 39b

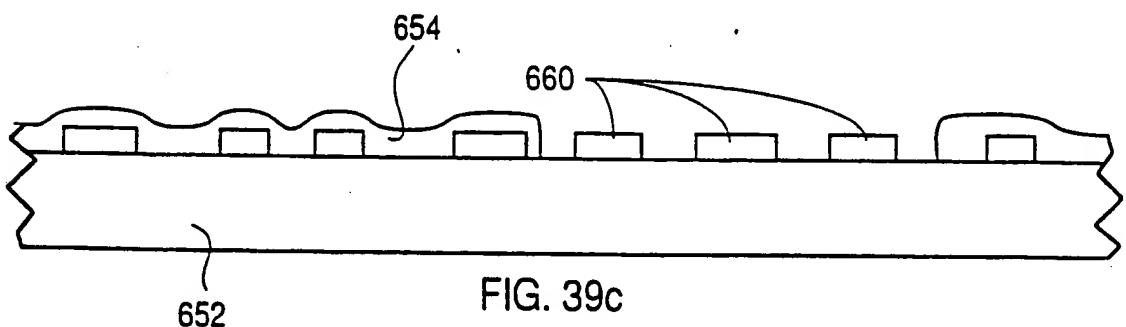


FIG. 39c

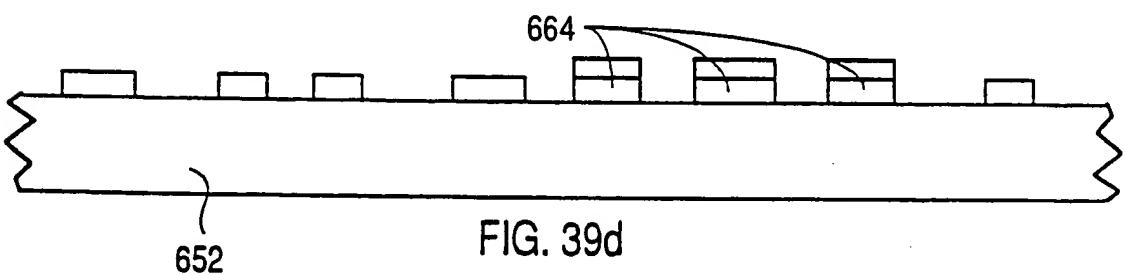
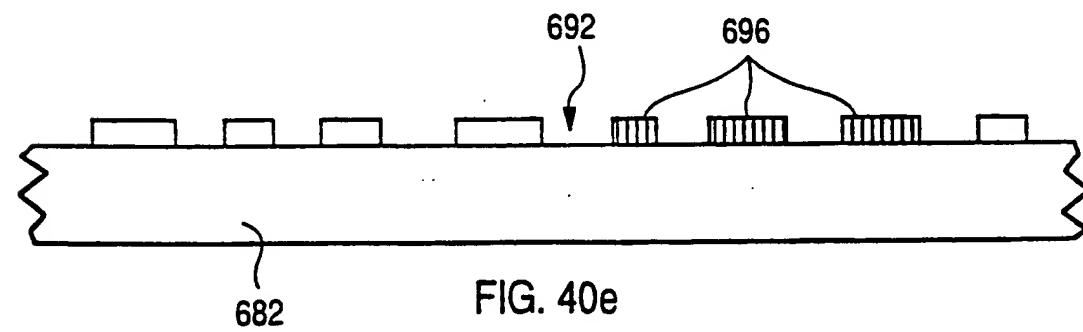
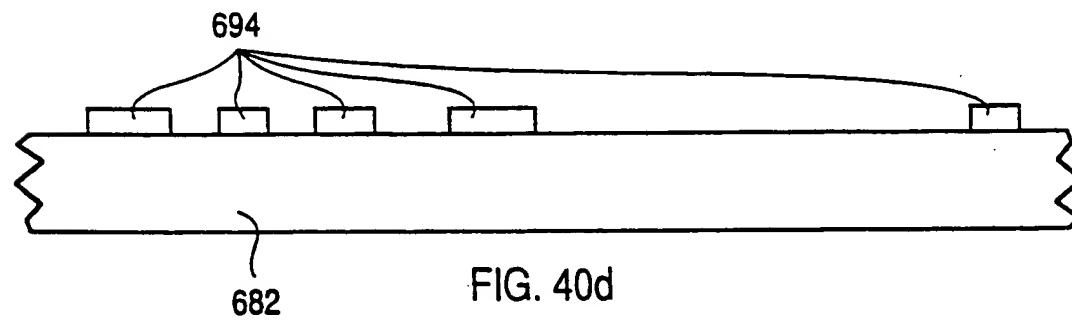
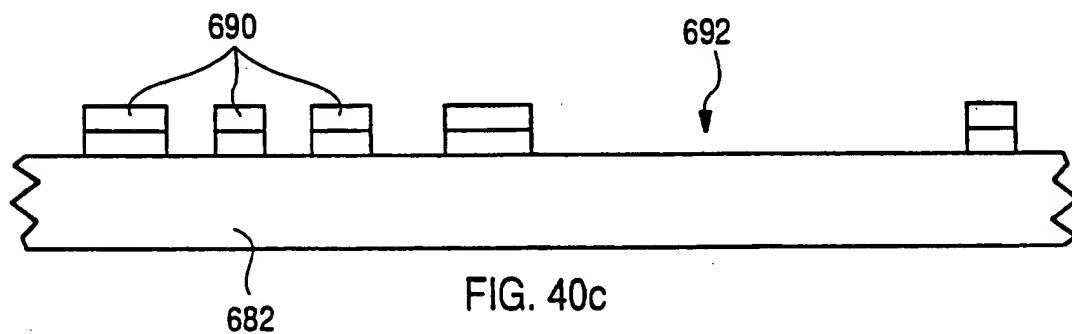
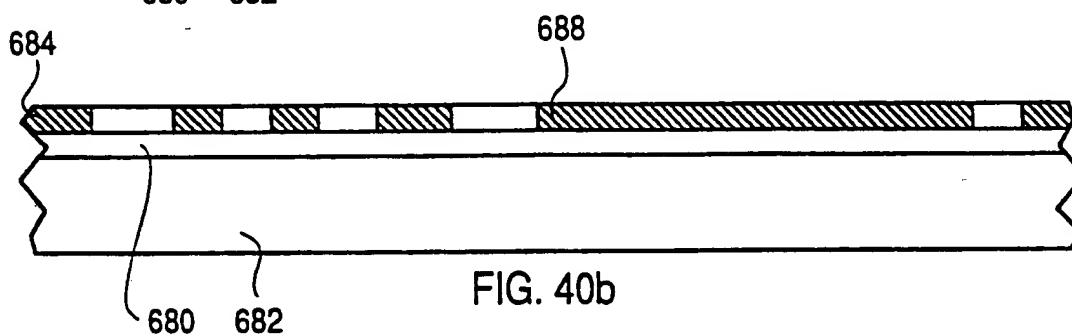
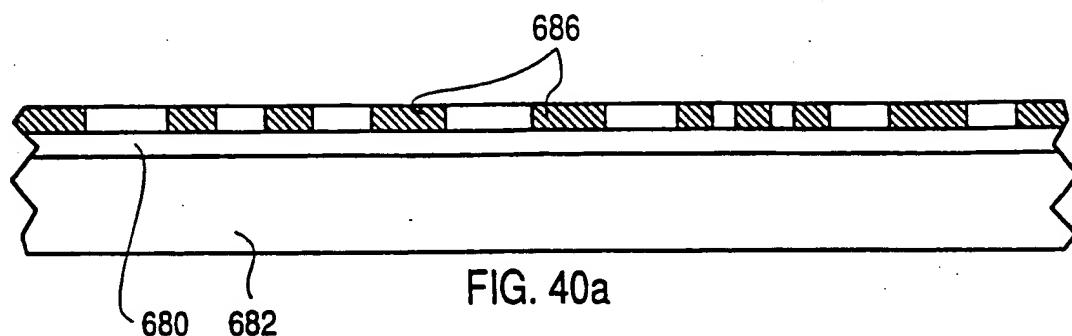


FIG. 39d

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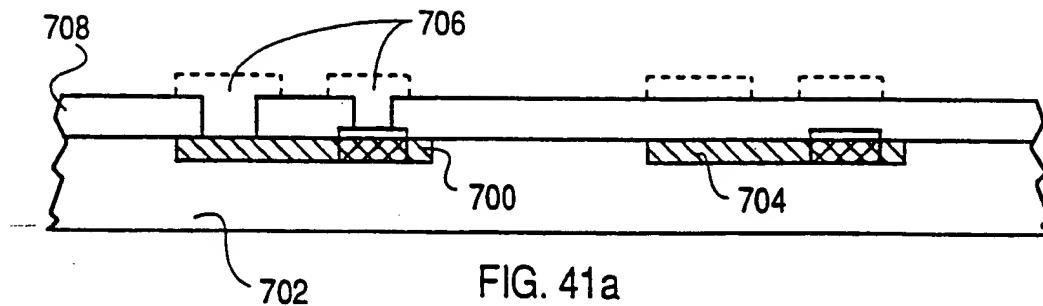


FIG. 41a

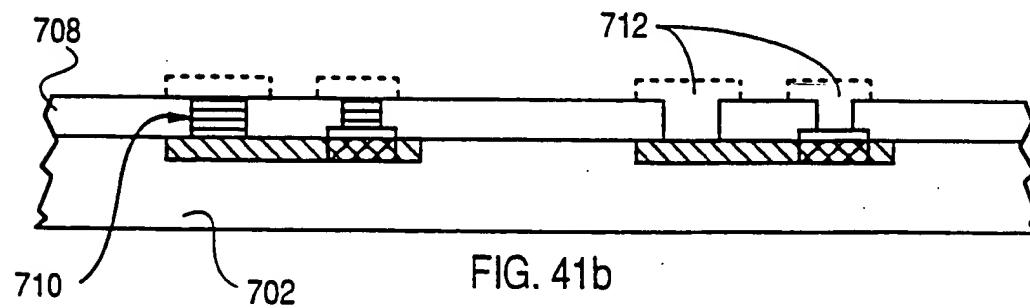


FIG. 41b

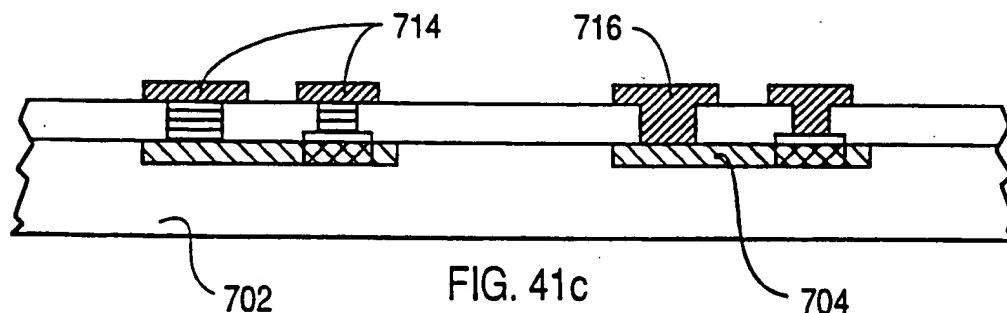
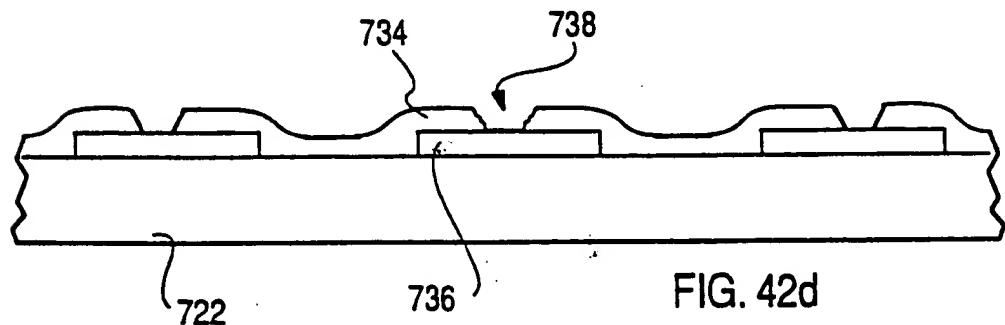
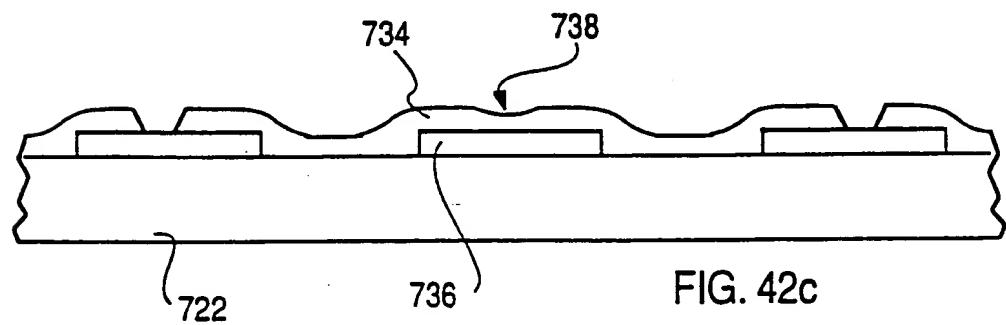
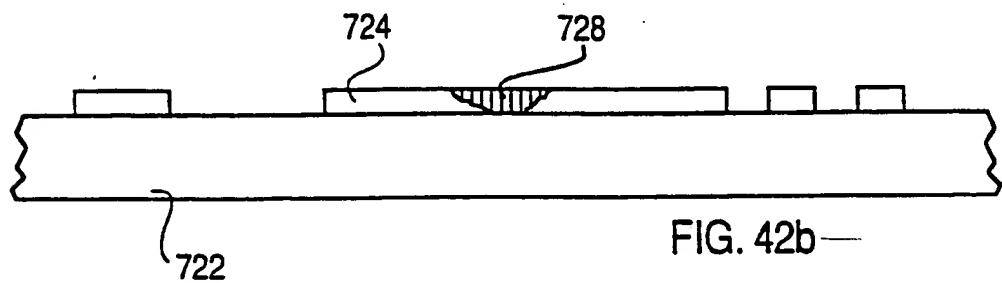
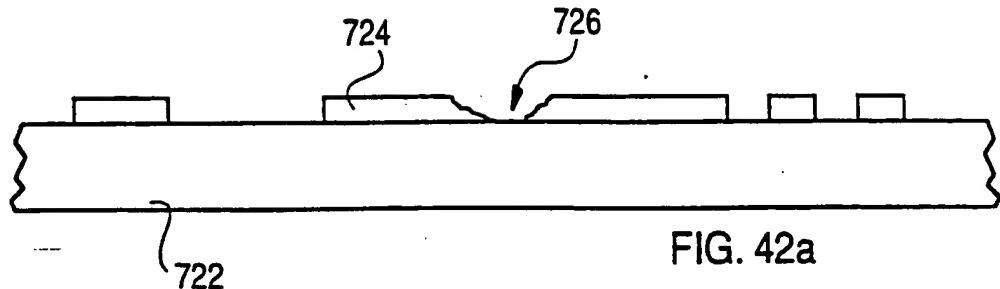


FIG. 41c

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# INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/01027

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) \*

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): H05K 3/30; B44C 1/22; G01R 1/04; B05D 5/12

## II. FIELDS SEARCHED

Minimum Documentation Searched ?

Classification System	Classification Symbols
US	29/825,047; 156/643 324/158F, 158P 427/97, 430/312 437/8,187

Documentation Searched other than Minimum Documentation  
to the Extent that such Documents are Included in the Fields Searched \*

## III. DOCUMENTS CONSIDERED TO BE RELEVANT \*

Category *	Citation of Document, ** with indication, where appropriate, of the relevant passages ***	Relevant to Claim No. 12
A	US, A, 3,405,361 08 October 1968 (L.E. Kattner et al.)	
Y	US, A, 3,618,201 09 November 1971 (Makimoto et al.)	1-5
A	US, A, 3,702,025 07 November 1972 (Archer)	
A	US, A, 4,038,599 26 July 1977 (Bove & Hubacher)	
A	US, A, 4,636,722 13 January 1987 (Ardezzone)	
X Y	US, A, 4,649,339 10 March 1987 (Grangroth & Loy)	6 7
Y	US, A, 4,820,976 11 April 1989 (Brown)	6-8
A	US, A, 4,853,627 01 August 1989 (Gleason et al.)	
A	US, Y, 4,585,727 29 April 1986 (Reams)	9
A	US, X, 4,868,068 19 September 1989 (Yamaguchi et al.)	37-38
X Y	Solid State Technology, May 1989, Jay Glanville, "Focused Ion Beam Technology for IC Modification" pages 270-272.	39 40

\* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

## IV. CERTIFICATION

Date of the Actual Completion of the International Search

08 JULY 1991

Date of Mailing of this International Search Report

11 JUL 1991

International Searching Authority

ISA/US

Signature of Authorized Officer

*André Rulman*  
CARL J. ARBES

## III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y	US, A, 4,983,250 08 January 1991 (Pan)	41
X	JP, A, 1-285946 16 November 1989 (Matu)	43
Y	JP, A, 53-76757 07 July 1978 (Kokai)	44
X	US, A, 4,564,584 14 January 1986 (Fredericks et al.)	45
X	US, A, 4,088,490 09 May 1978 (Duke et al.)	46
Y	US, A, 4,115,120 19 September 1978 (dryer et al.)	47
A	US, A, 4,936,950 26 June 1990 (Doan et al.)	48-49
A	US, A, 259,163 09 March 1988 (Rath)	37-40
A	EP, A, 259,162 09 March 1988 (Creedon)	51-54
X	US, A, 4,409,139 11 October 1983 (Colacino et al.)	51-54
Y	US, A, 3,905,818 16 September 1975 (Margrain)	37-38
Y	US, A, 4,764,485 16 August 1988 (Loughran et al.)	41